

Compal confidential

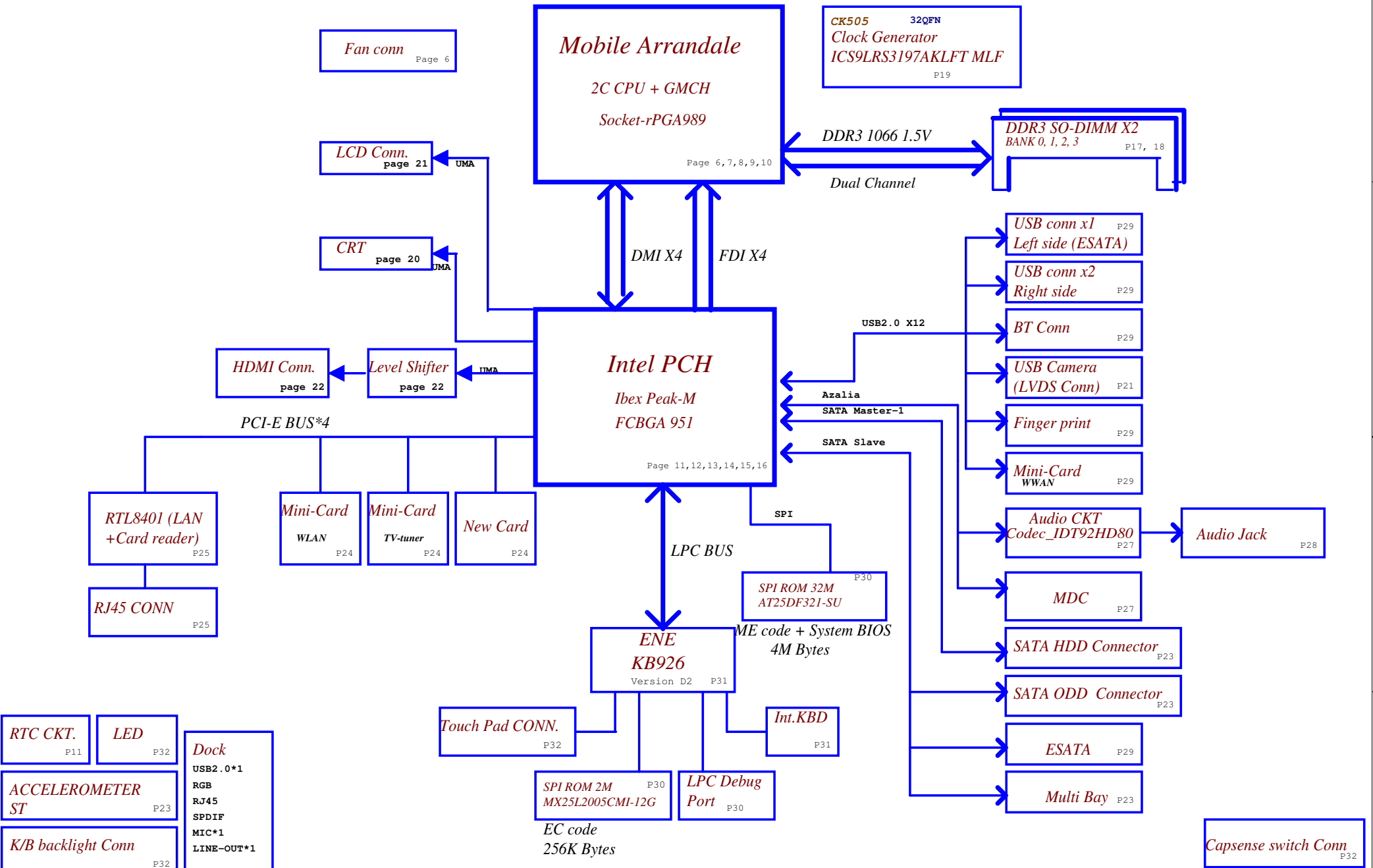
Schematics Document

Mobile Arrandale rPGA989 with
Intel PCH(Ibex Peak-M) core logic

2009-11-05

Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/28	Deciphered Date	2006/03/10	Cover Sheet	
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				Date: Thursday, November 12, 2009	Rev 1.0
				Sheet 1	5

Calpella Consumer 14" UMA



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Issued Date		2006/02/13		Deciphered Date		2006/03/10		Title		
								Block Diagram		
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Voltage Rails

O MEANS ON X MEANS OFF

power plane State	+B VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +1.05VS +1.5VS_CPU
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	XDP	BATT	Thermal Sensor	SODIMM	CLK GEN	WWAN	WLAN	M93 Thermal Sensor	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	X	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	PCH	X	X	X	V	V	V	V	X	X	V	V
SML0CLK SML0DATA	PCH	X	X	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH	X	X	X	X	X	X	X	X	X	X	X
VCCP		+3VS			+3VS	+3VS	+3VS @+3VALW	+3VS @+3VALW	+3VL		+3VS	+3VS

ZZZ

DAZ0BI00100
PA@

DAZ0BI00400
OPP@

PCB: DA60000F400
PA@: DAZ0BI00600 (w/o SIM daughter/B)
OPP@: DAZ0BI00400

Symbol Note :



: means Digital Ground

: means Analog Ground

@ : means just reserve , no build

45@ : means need be mounted when 45 level assy or rework stage.

BATT @ : means need be mounted when 45 level assy or rework stage.

CONN@ : means ME part

PA@ : Only For PA (With Capacitor sensor)

OPP@ : For POWER BUTTON (NO CAP SERSOR)

DEBUG@ : For DEBUG

USB assignment:

USB-0	Left side(with ESATA)
USB-1	Right side
USB-2	Right side
USB-3	Dock
USB-4	Camera
USB-5	MiniCard(WLAN)
USB-6	X (HM55 don't support)
USB-7	X (HM55 don't support)
USB-8	MiniCard(WWAN)
USB-9	New Card
USB-10	X
USB-11	Finger Printer
USB-12	Bluetooth
USB-13	X

PCIe assignment:

PCle-1	WWAN
PCle-2	WLAN
PCle-3	RTL8401 Combo
PCle-4	New card
PCle-5	X
PCle-6	X
PCle-7	X (HM55 don't support)
PCle-8	X (HM55 don't support)

SATA assignment:

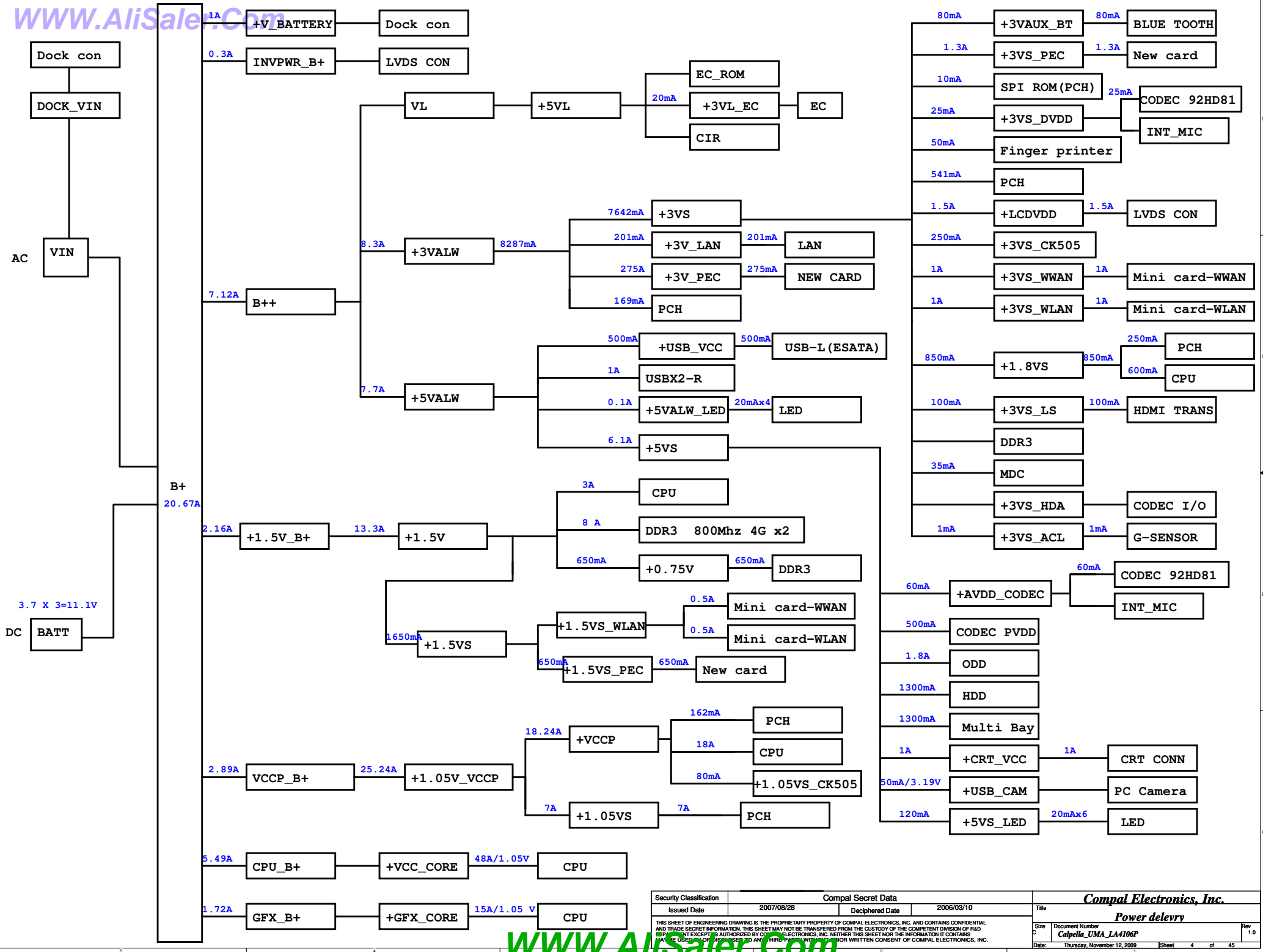
SATA0	HDD
SATA1	ODD
SATA2	X (HM55 don't support)
SATA3	X (HM55 don't support)
SATA4	ESATA
SATA5	Multi Bay

PCH I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0
G sensor	1D	0 0 0 1 1 1 0 1

EC I2C / SMBUS1 ADDRESSING

DEVICE	HEX	ADDRESS
Smart Battery		
Cap Sensor board		



Calpella UMA power on sequence(AC mode)

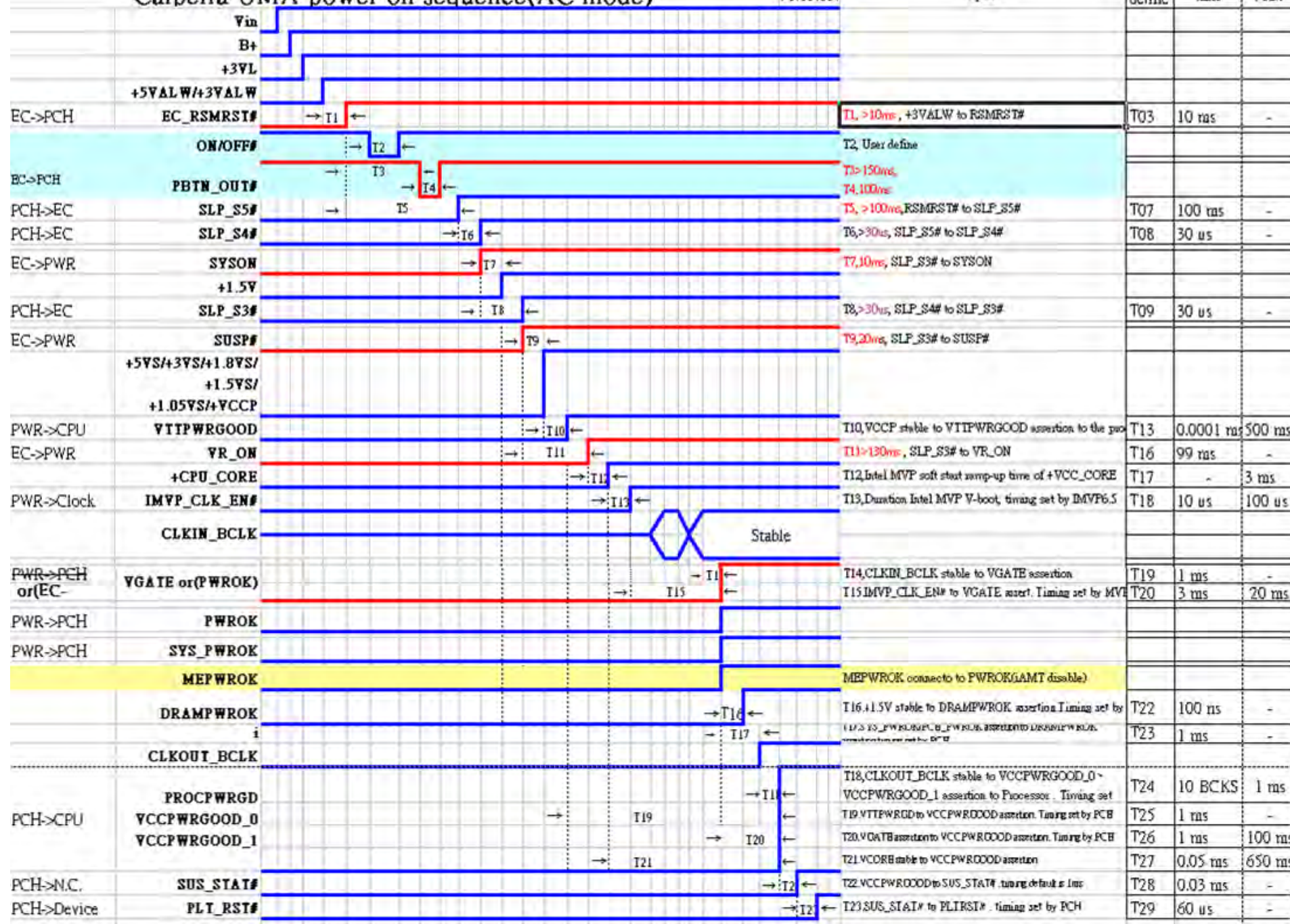
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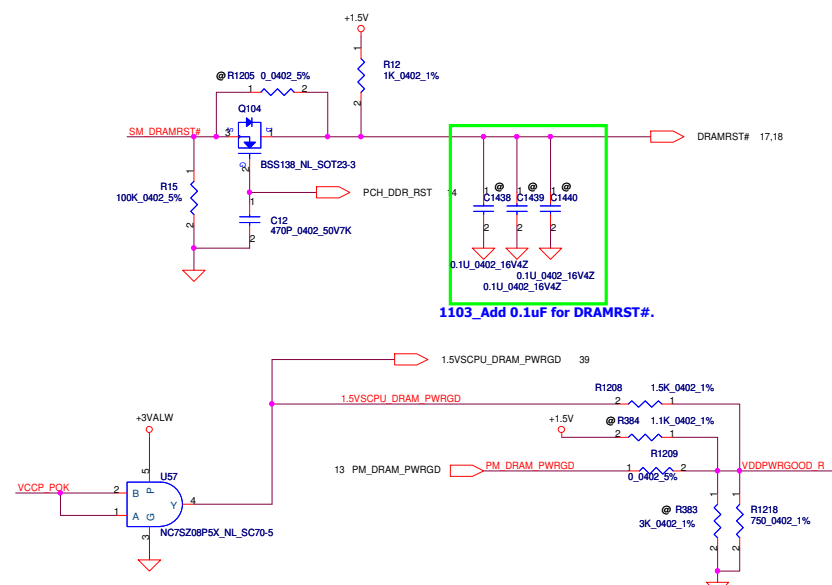
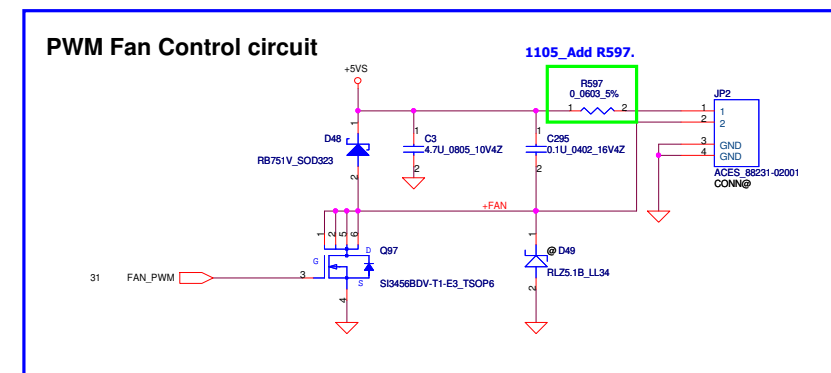
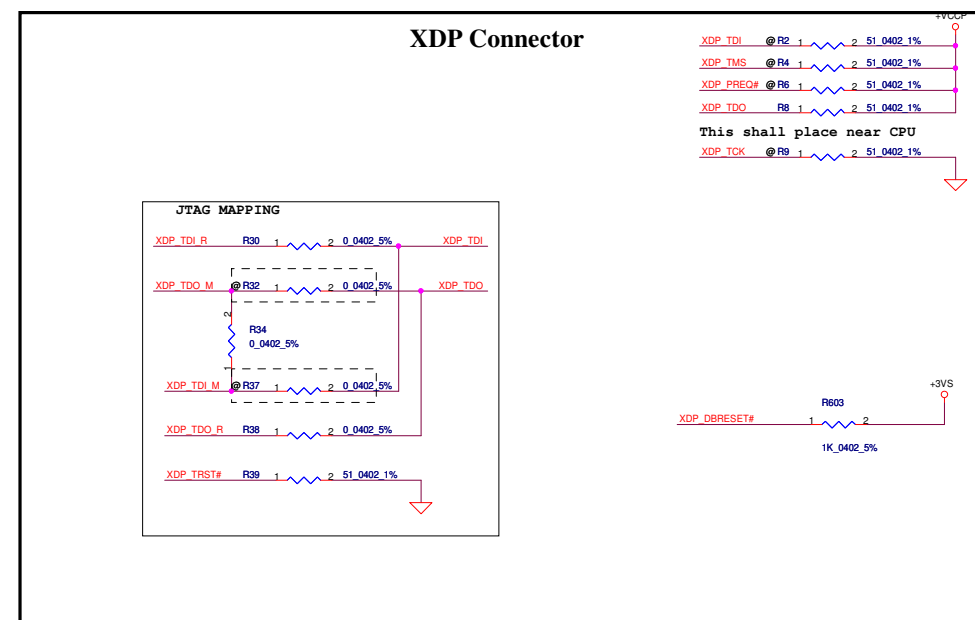
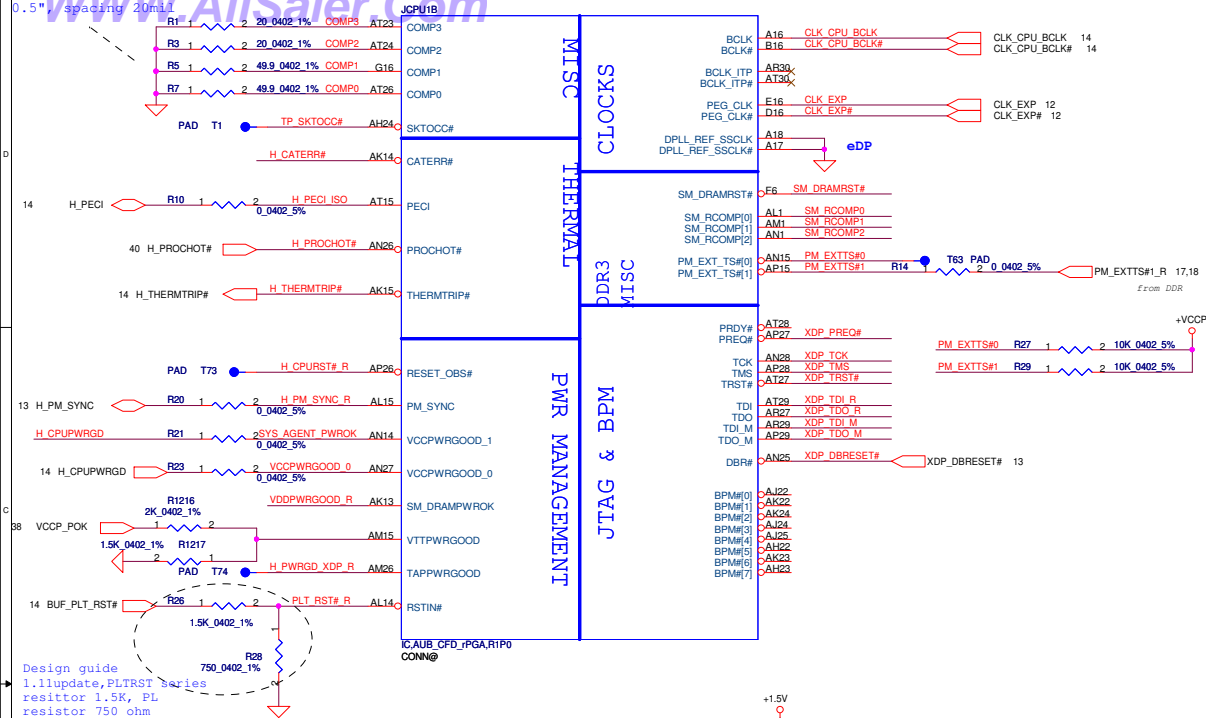
Spec

define

min

Max



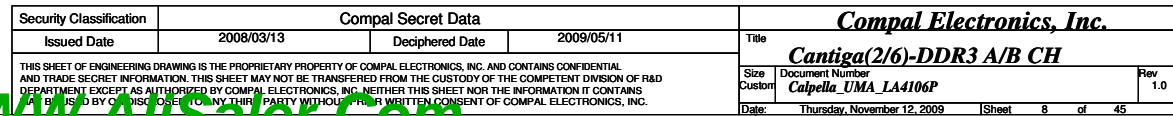


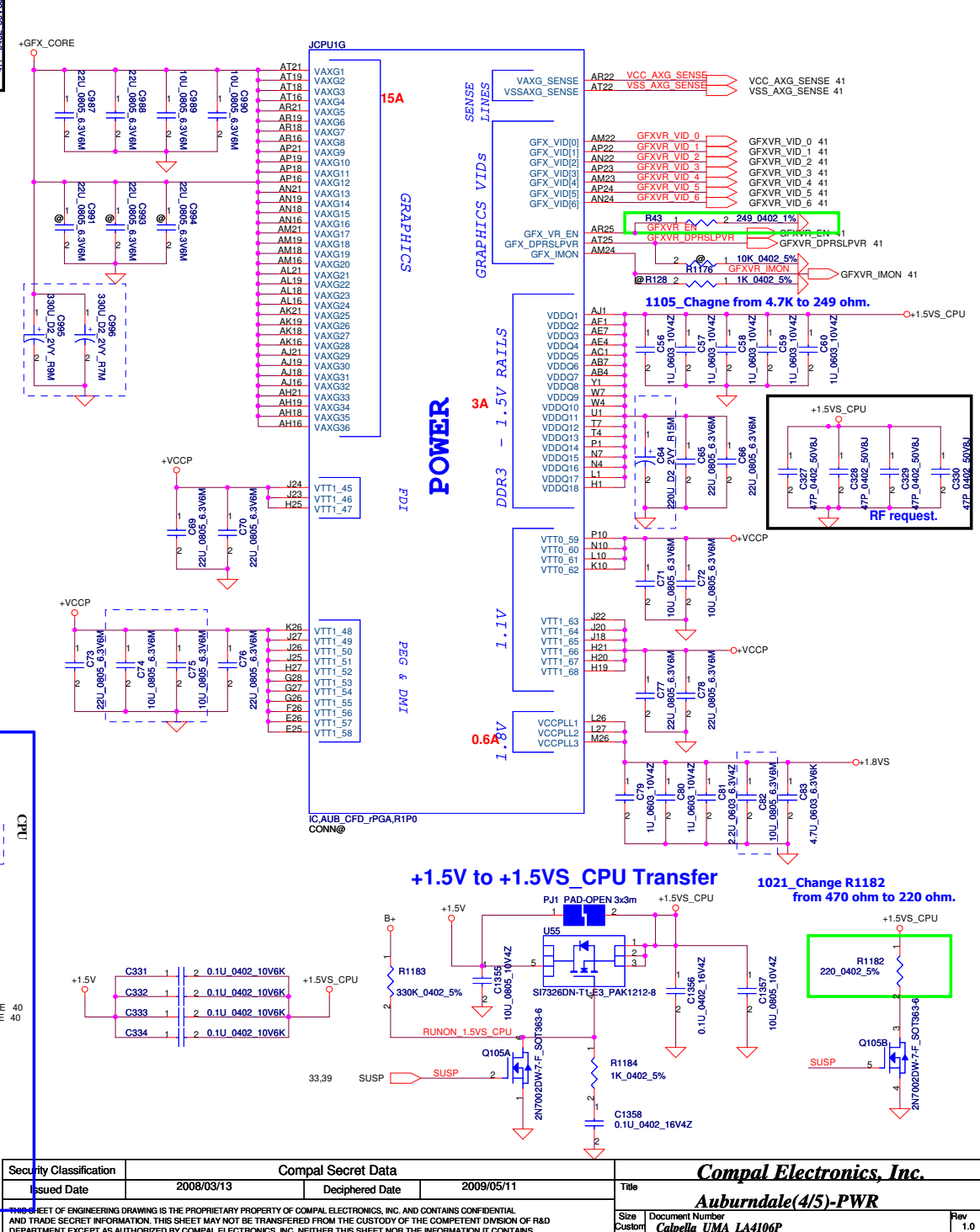
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Issued Date	2008/03/13	Deciphered Date	2009/05/11	Title	Auburndale(1/5)-Thermal/XDP	
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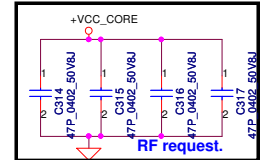
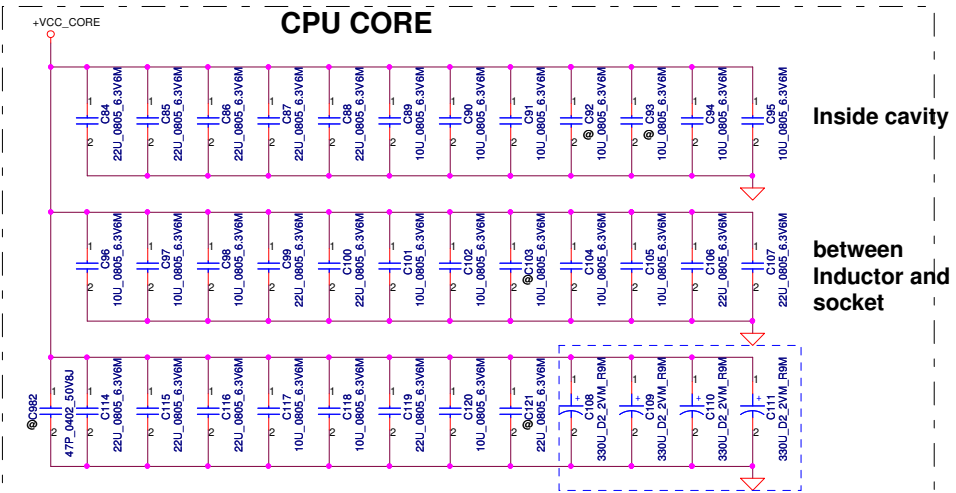
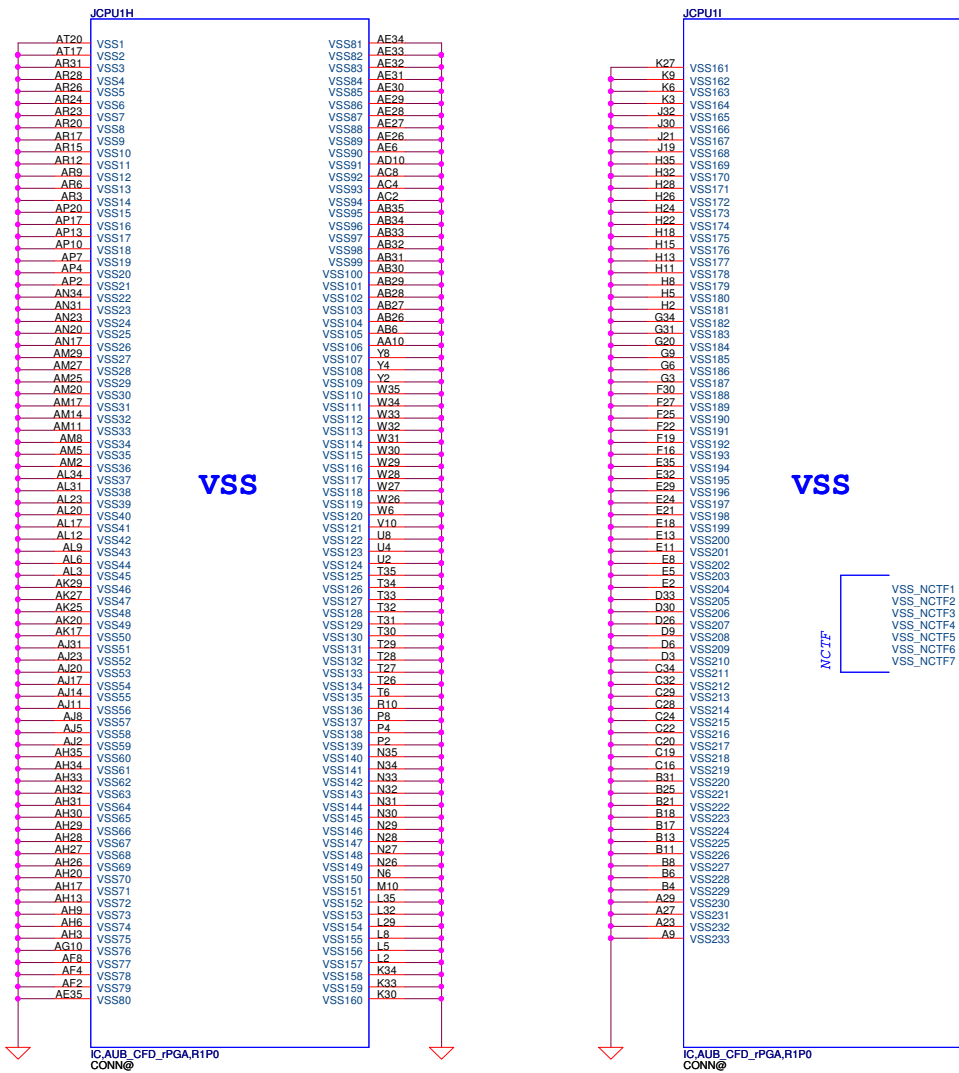


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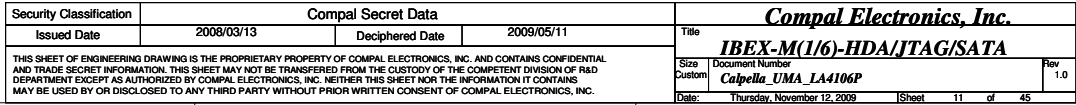
Compal Electronics, Inc.			
Title Auburndale(2/5)-DMI/PEG/FDI			
Size Custom	Document Number Calpella_UMA_LA4106P		Rev 1.0
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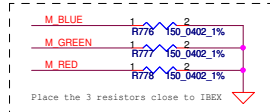
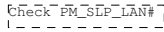




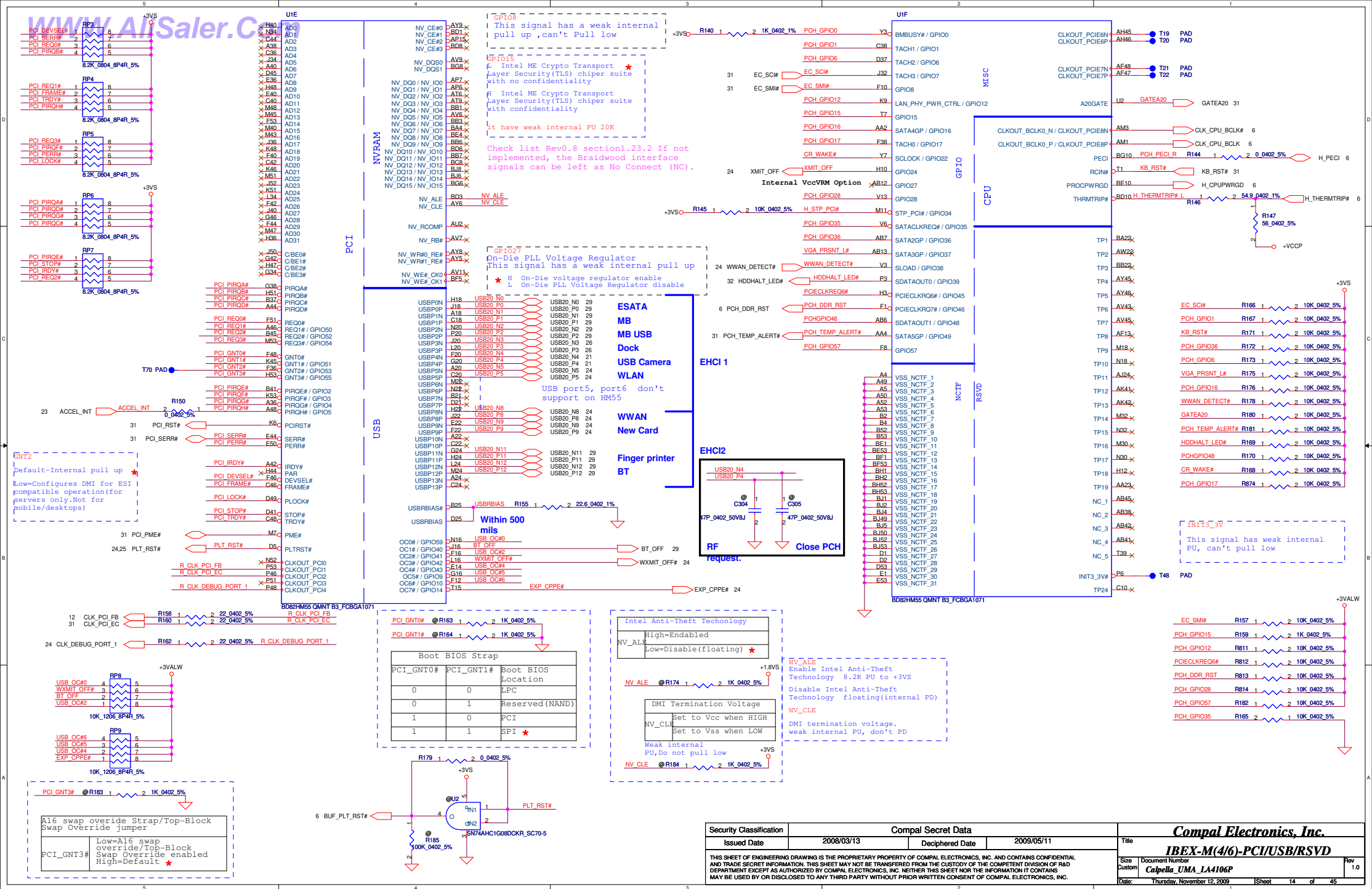
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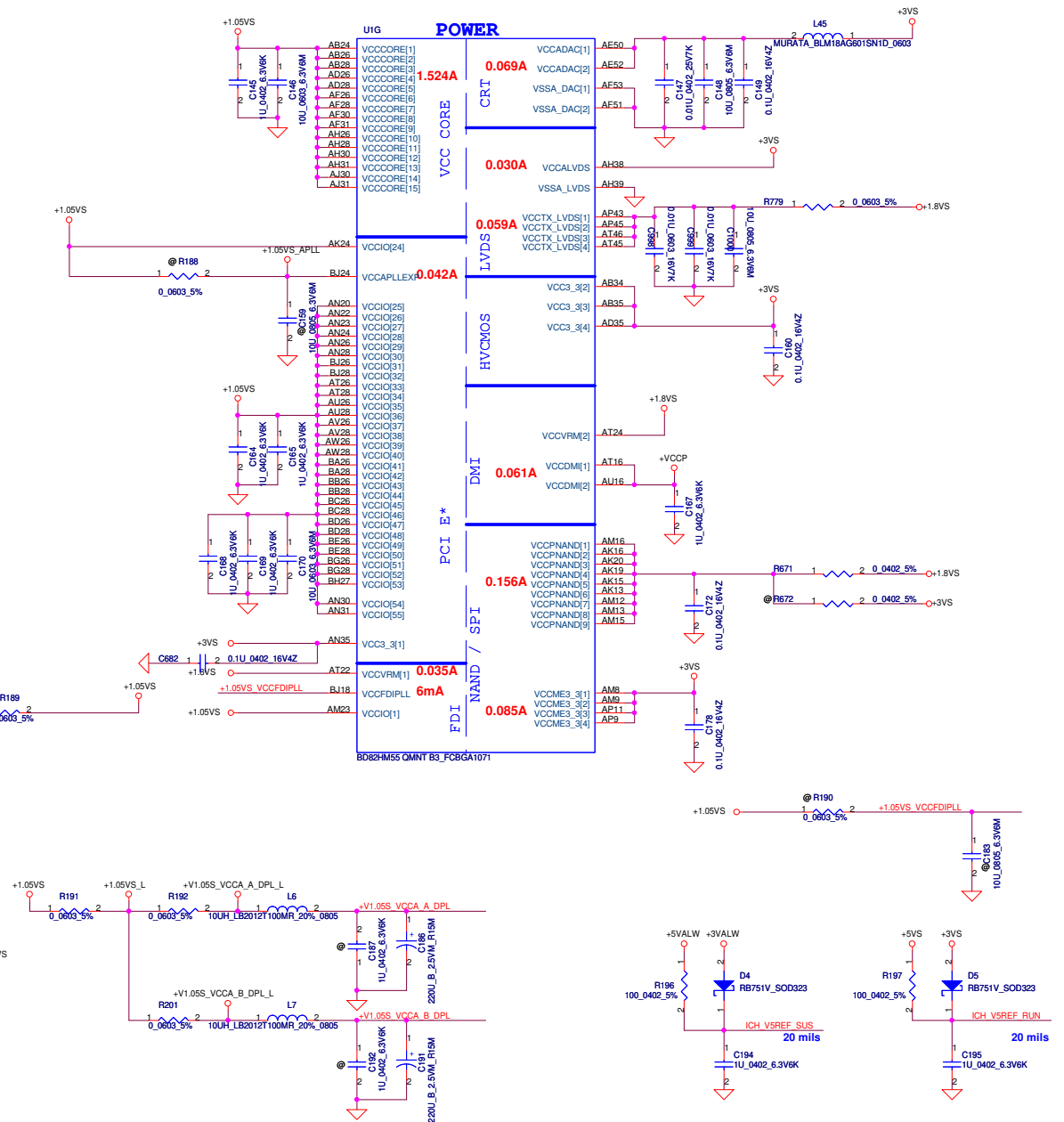




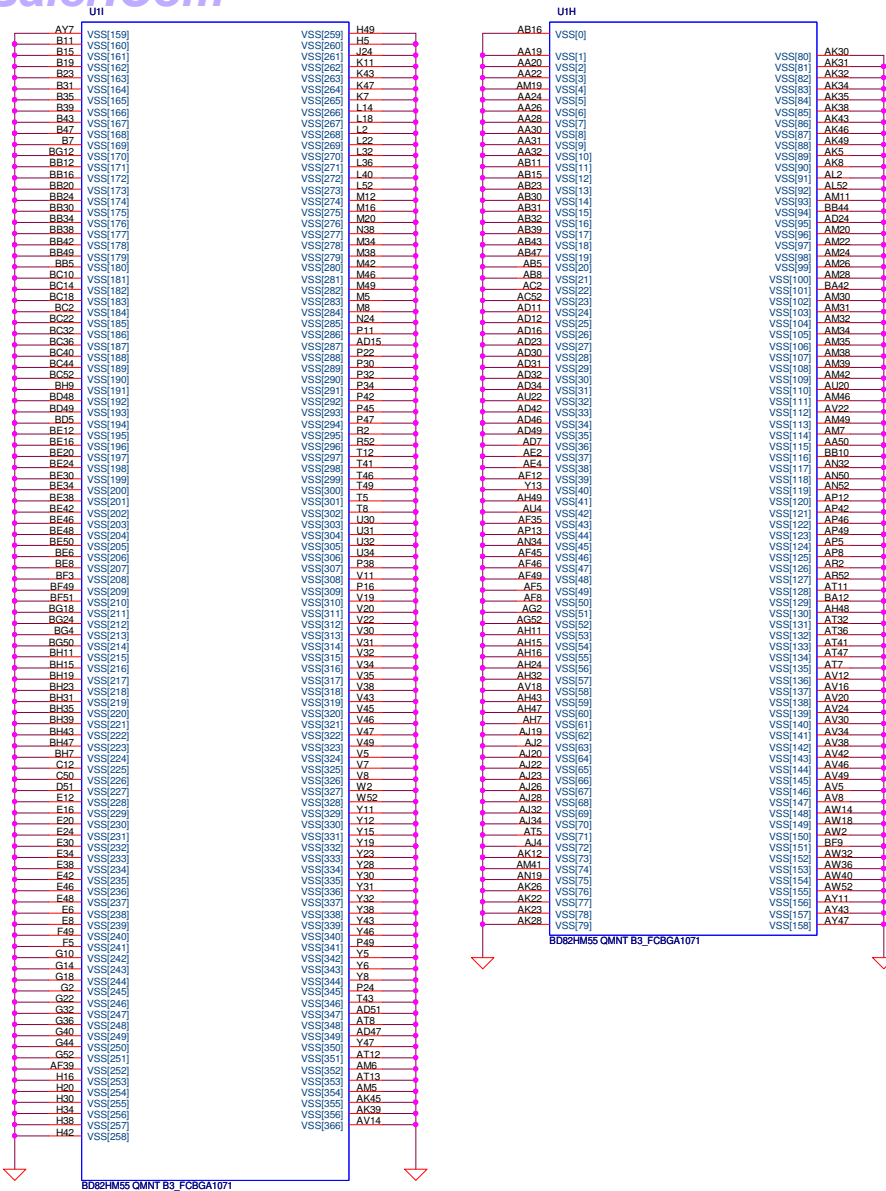


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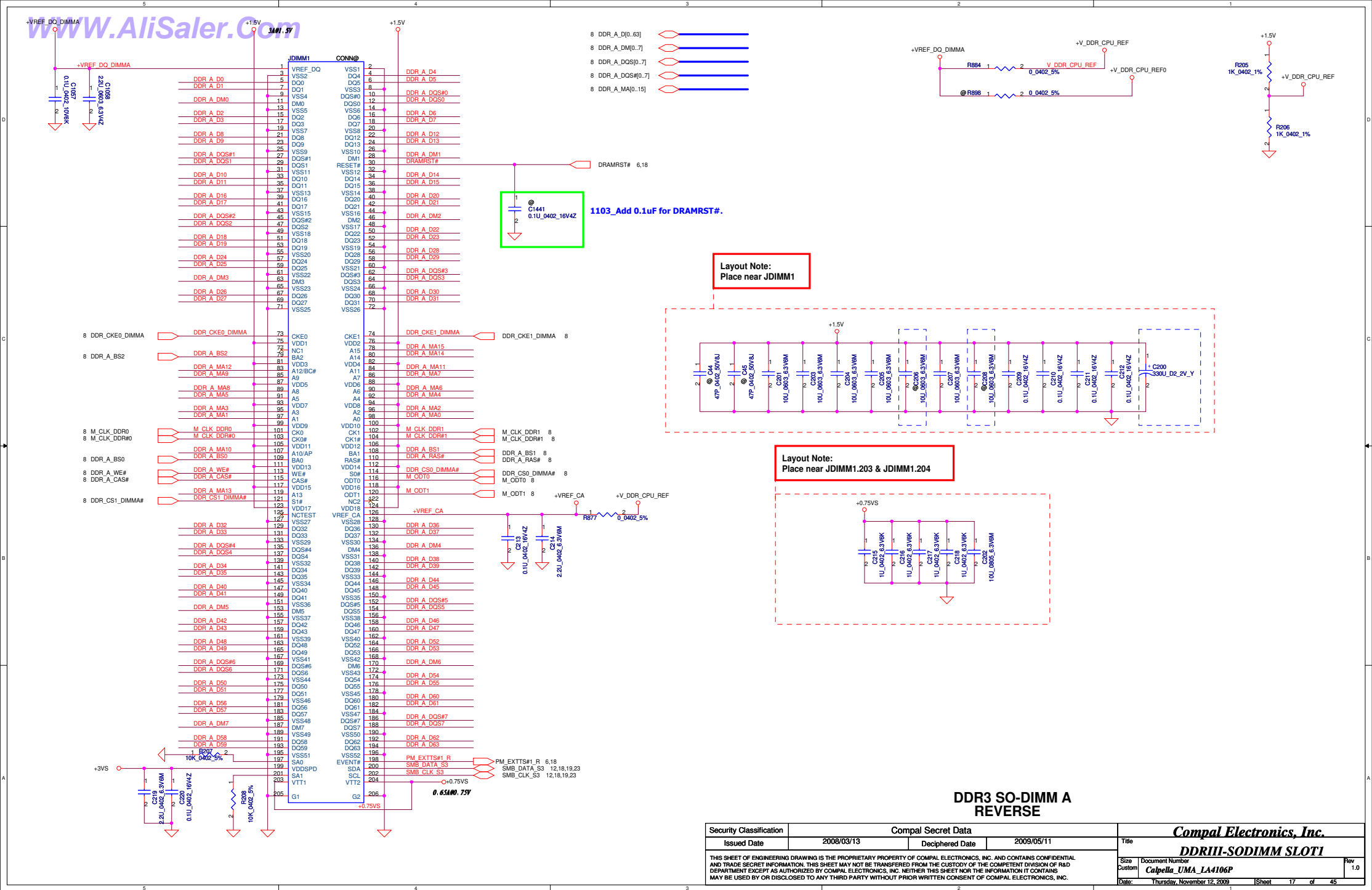


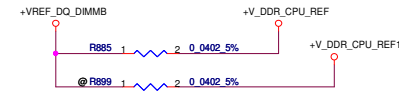
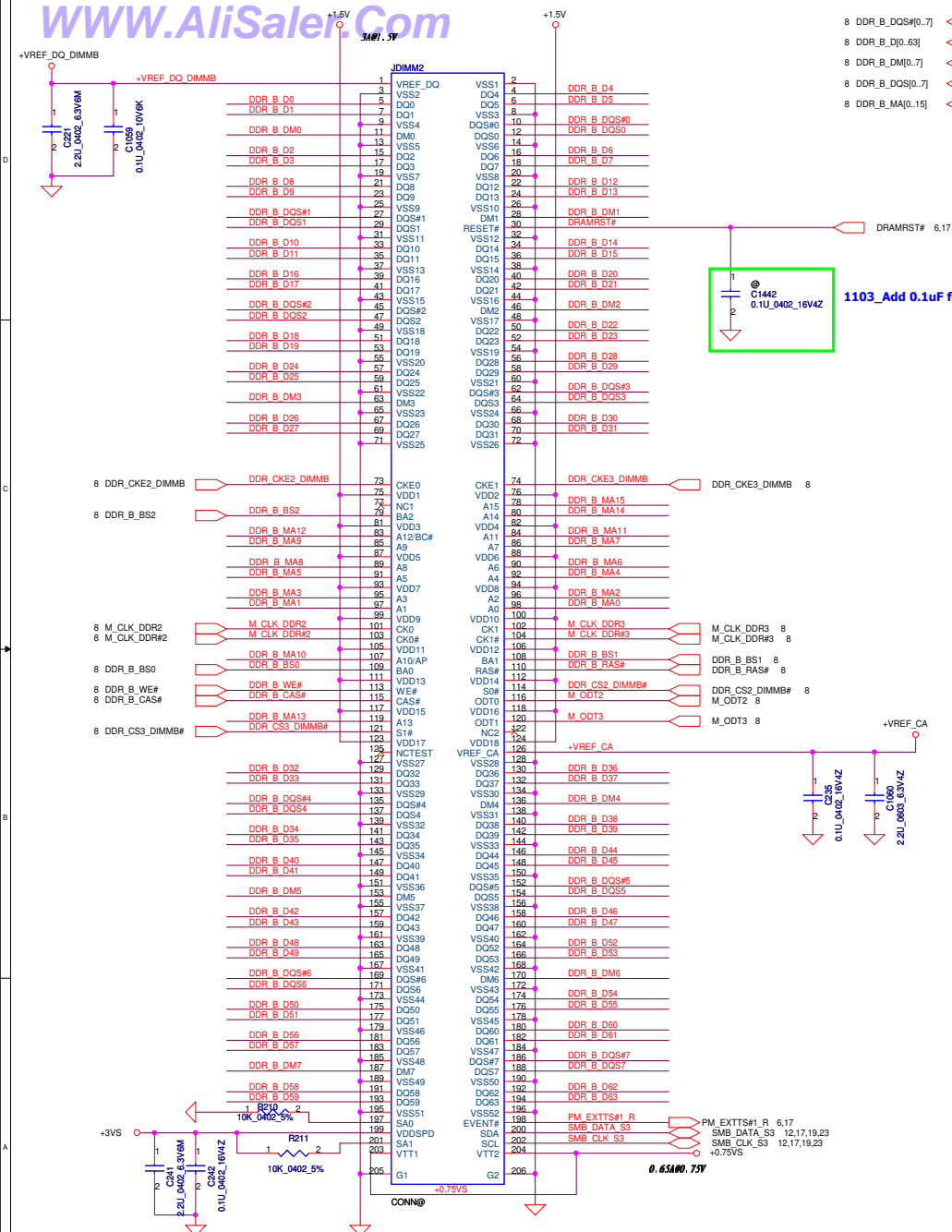


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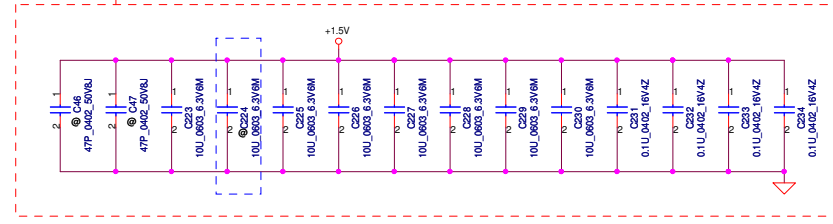
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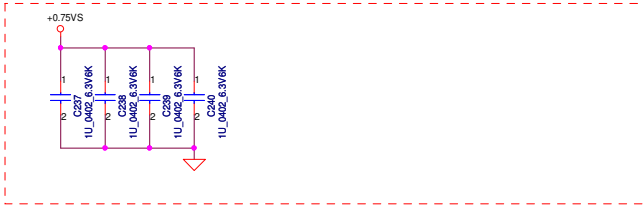


1103_Add 0.1uF for DRAMRST#.

Layout Note:
Place near JDIMM2

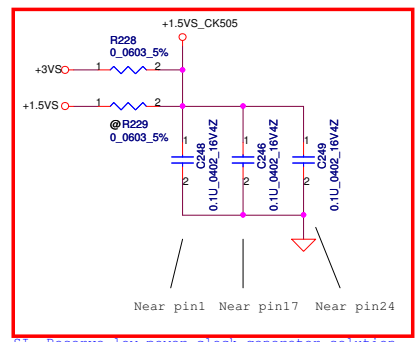


Layout Note:
Place near JDIMM2.203 & JDIMM2.204



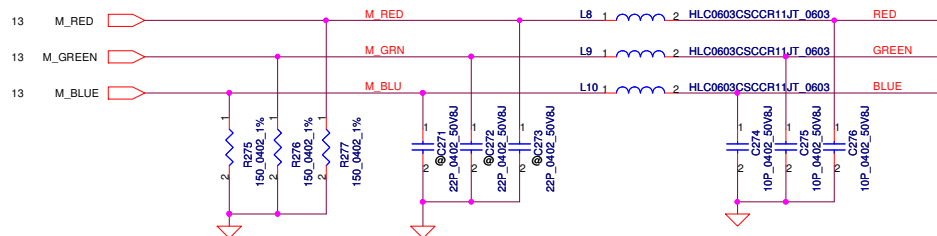
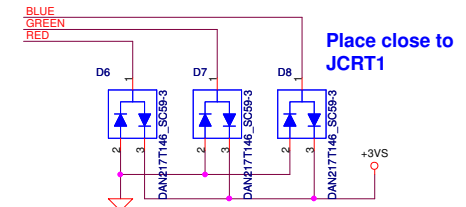
DDR3 SO-DIMM B
REVERSE

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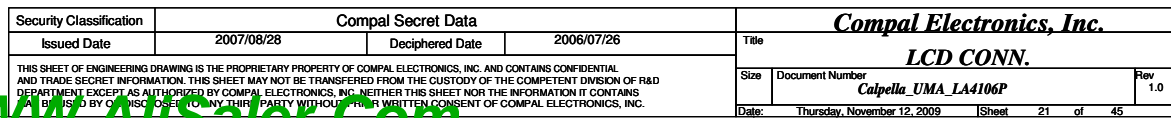


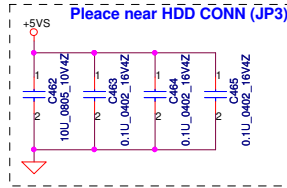
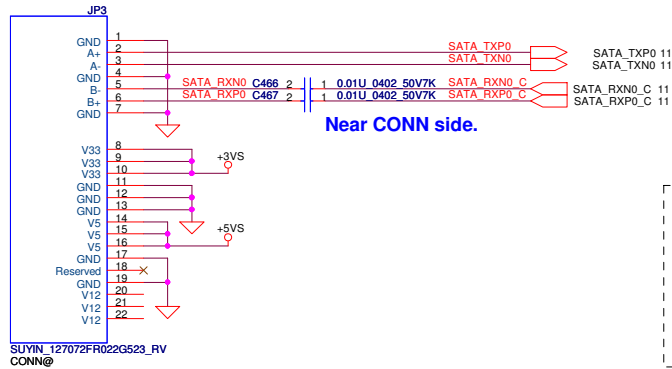
PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1	100MHz	100MHz

The diagram shows the connection for the REF0/CPU_SEL pin. A +3VS supply is connected to the top of two resistors, R244 and R247. The bottom of both resistors is connected to ground. The output of the resistors is connected to the REF0/CPU_SEL pin.

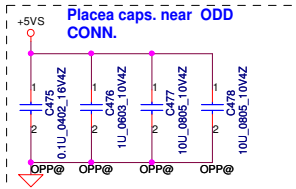
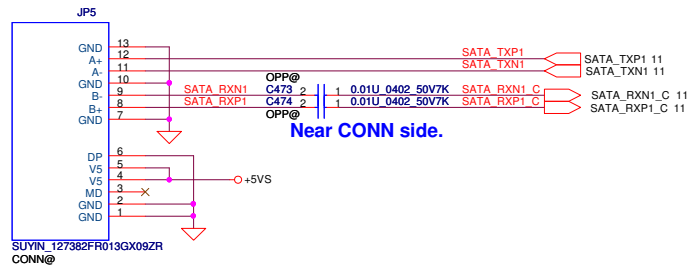


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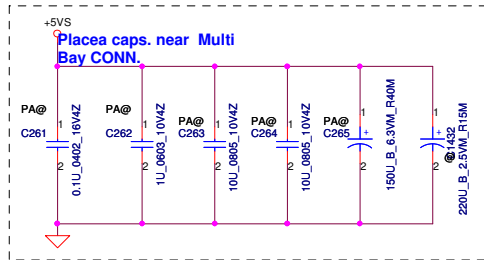
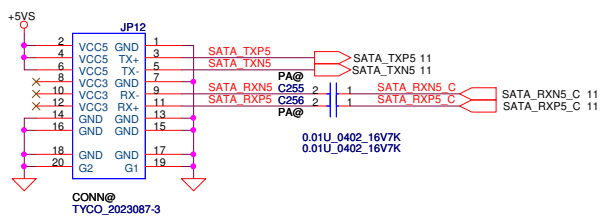




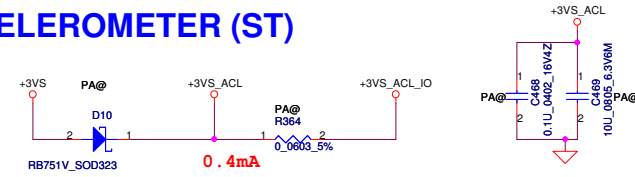
CD-ROM Connector



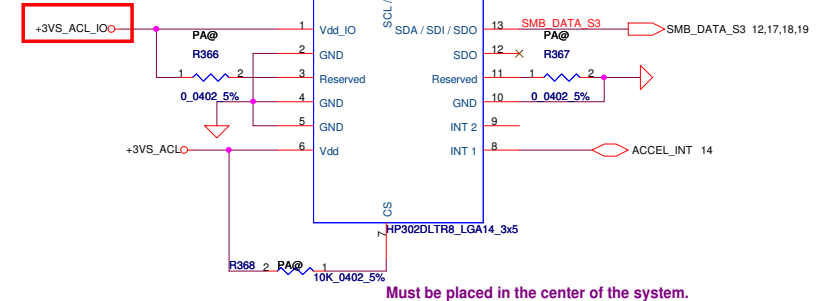
Multi Bay



ACCELEROMETER (ST)

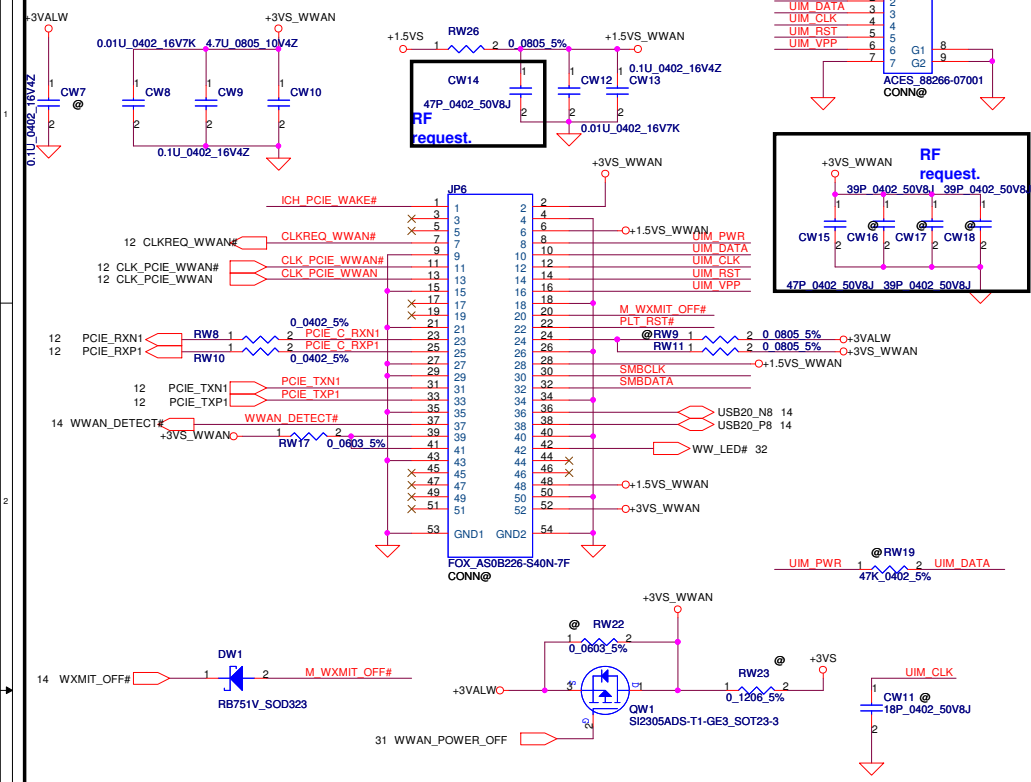


VDDIO absolute man
rating is VDD+0.1

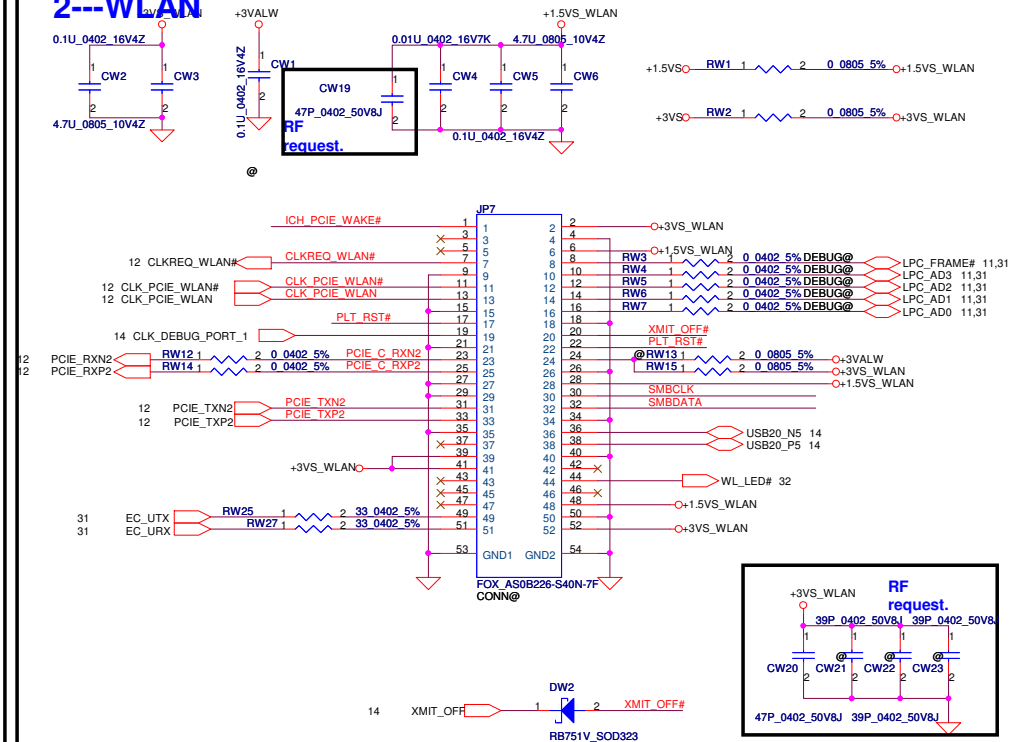


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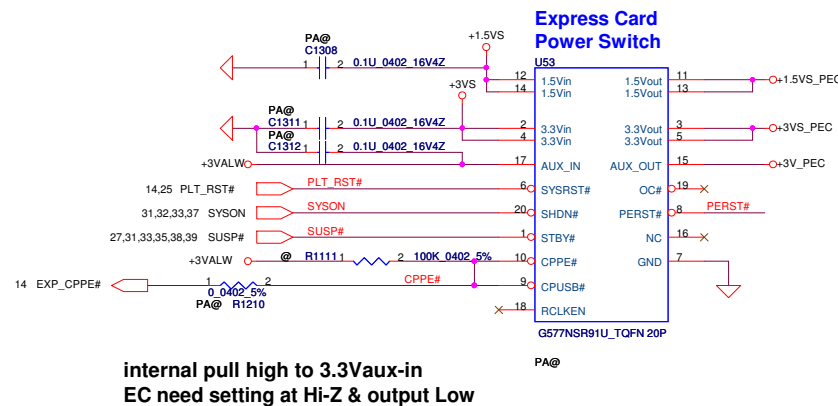
**Mini Card 0--TV
tuner/WWAN/Robson**



Mini Card

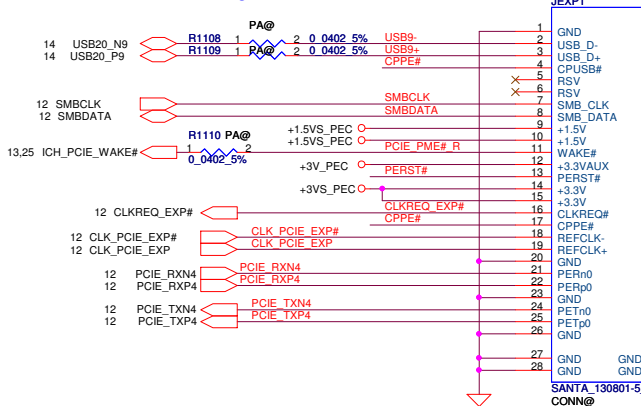


New Card

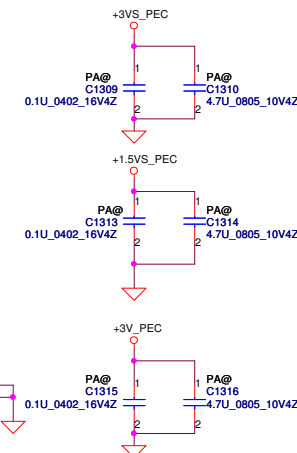


internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low

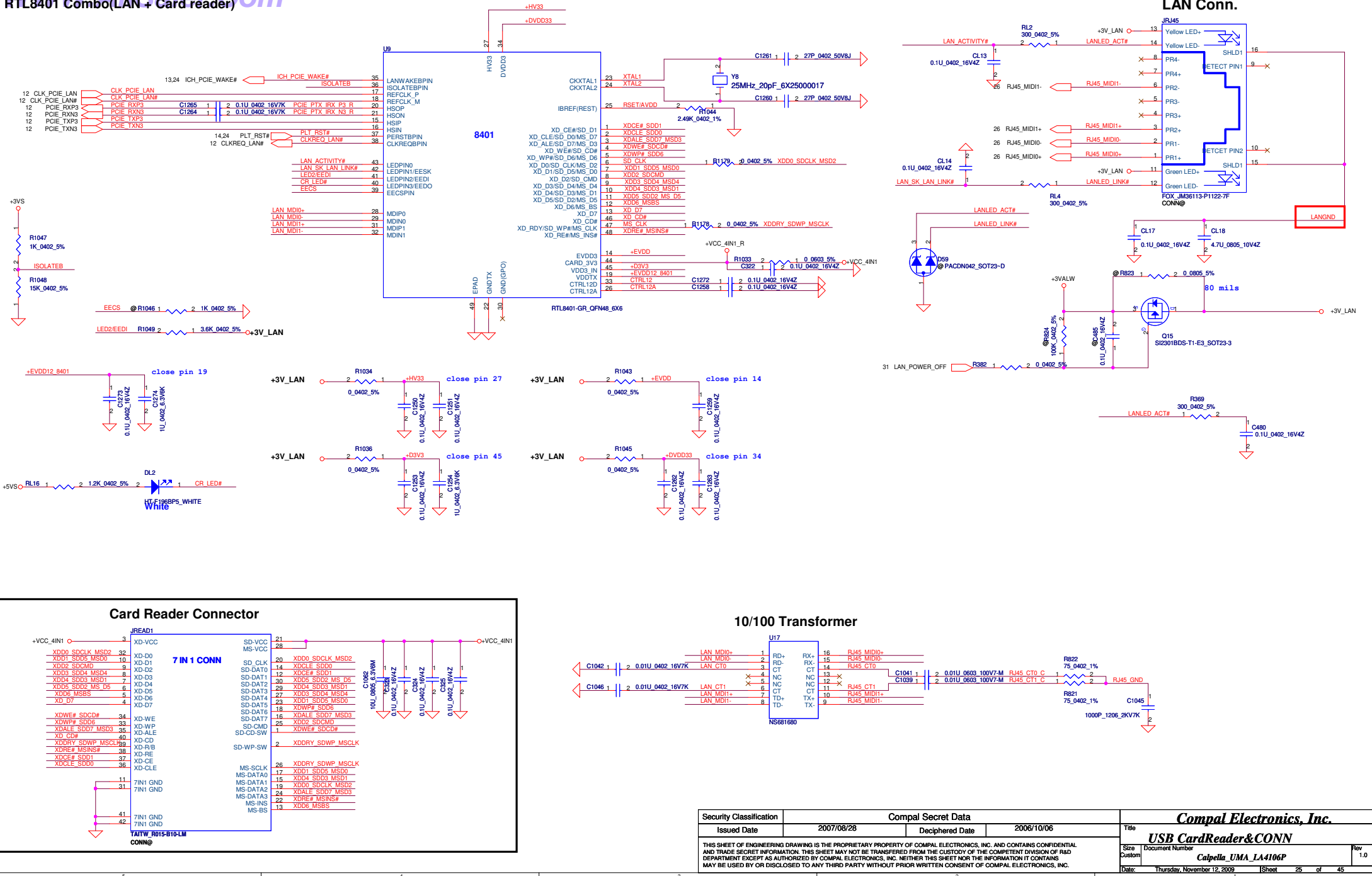
Close to
JEXP

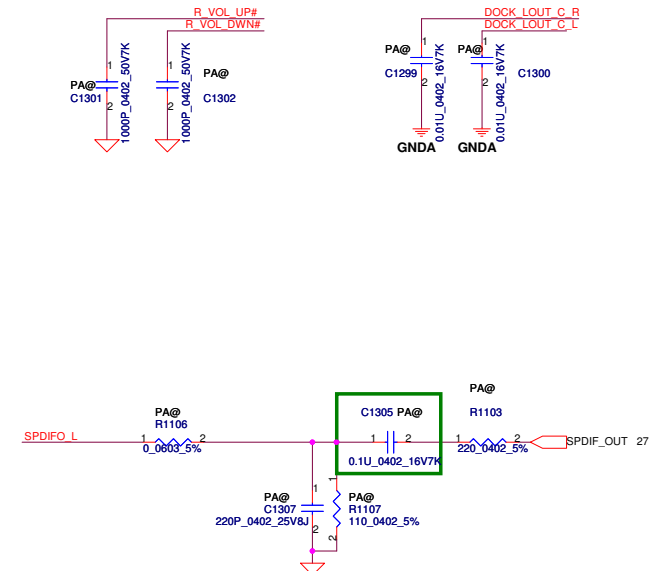
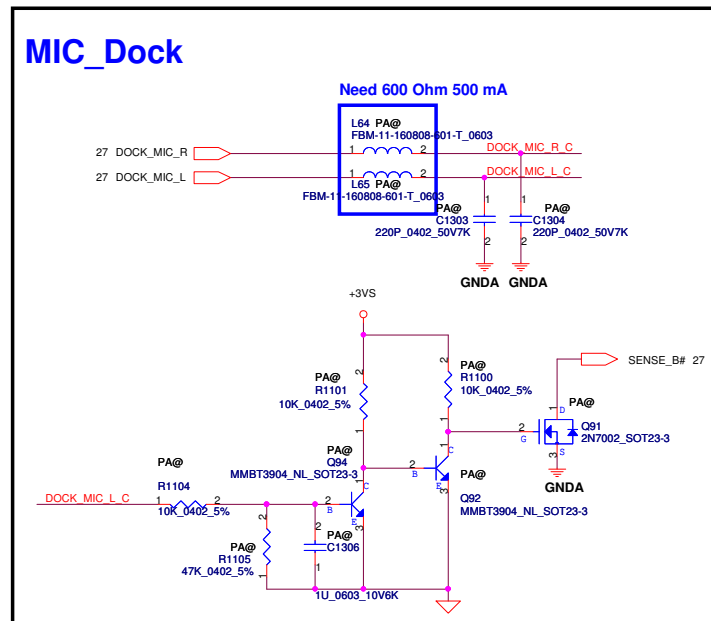
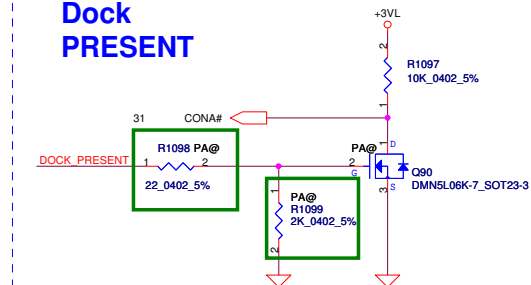
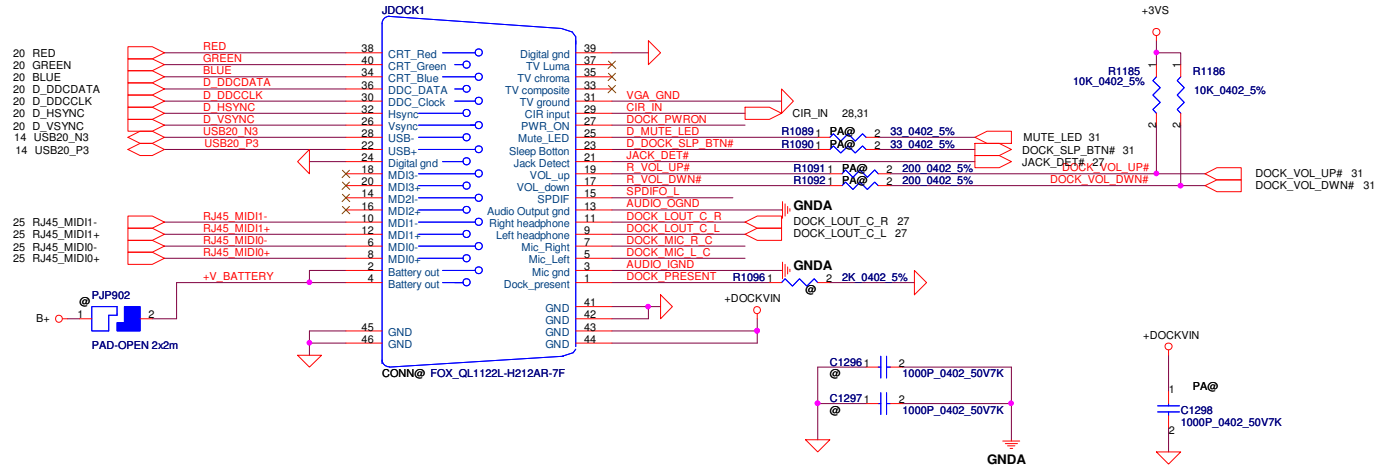


Near to Express Card slot.



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1105_Reserve the others +5VS power for Codec.

1102_Reserve 4.7uF.

1102_Reserve LDO power for Codec.

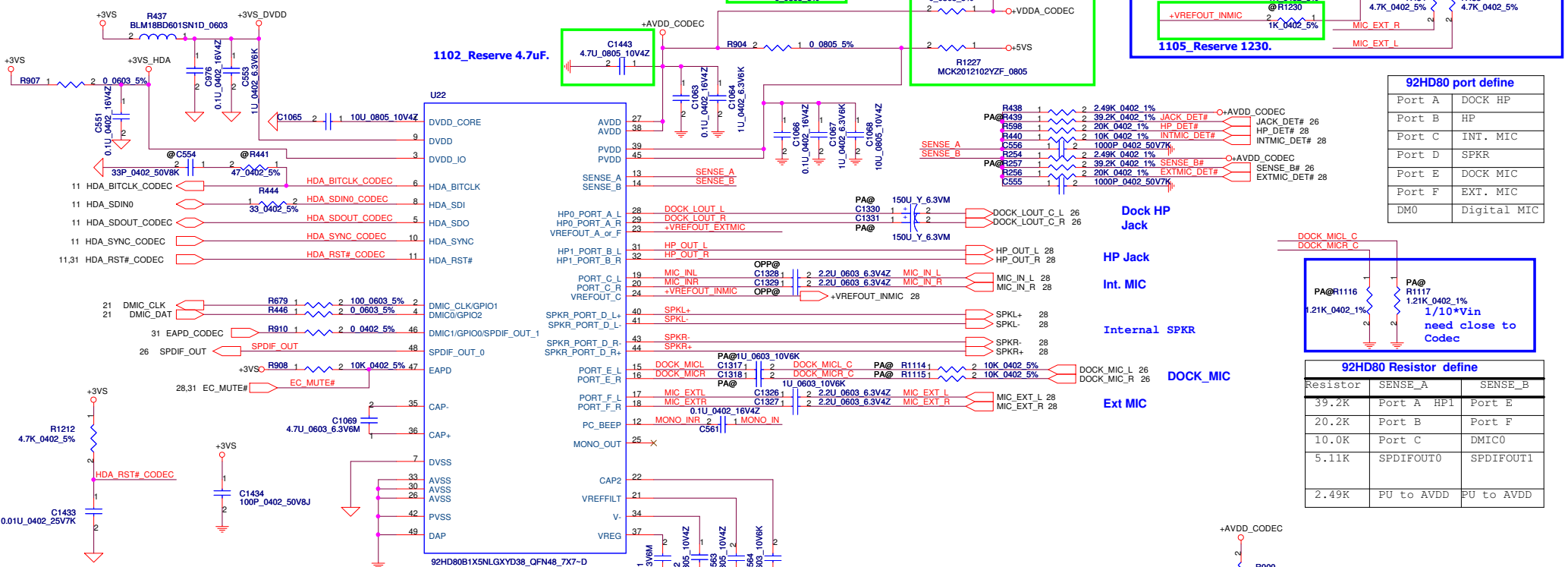
1105_Reserve 1230.

92HD80 port define

Port A	DOCK HP
Port B	HP
Port C	INT. MIC
Port D	SPKR
Port E	DOCK MIC
Port F	EXT. MIC
DM0	Digital MIC

92HD80 Resistor define

Resistor	SENSE_A	SENSE_B
39.2K	Port A HP1	Port E
20.2K	Port B	Port F
10.0K	Port C	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1
2.49K	PU to AVDD	PU to AVDD

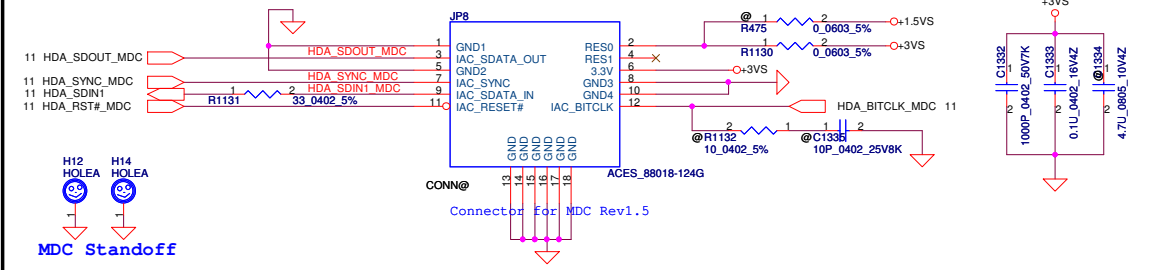


CODEC POWER

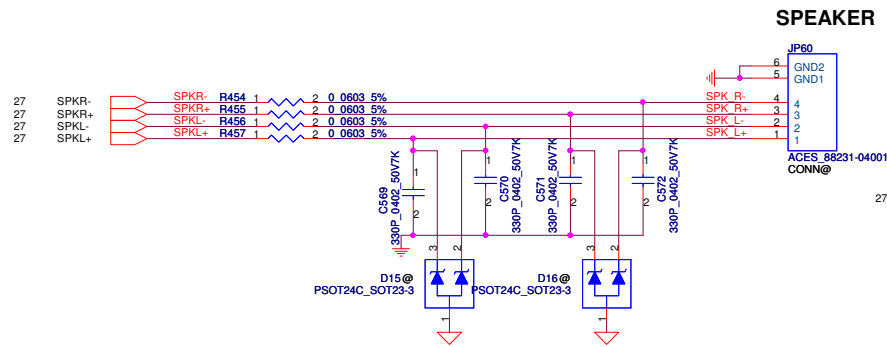
(4.75V)
300mA

1102_Reserve CODEC LDO for Codec.

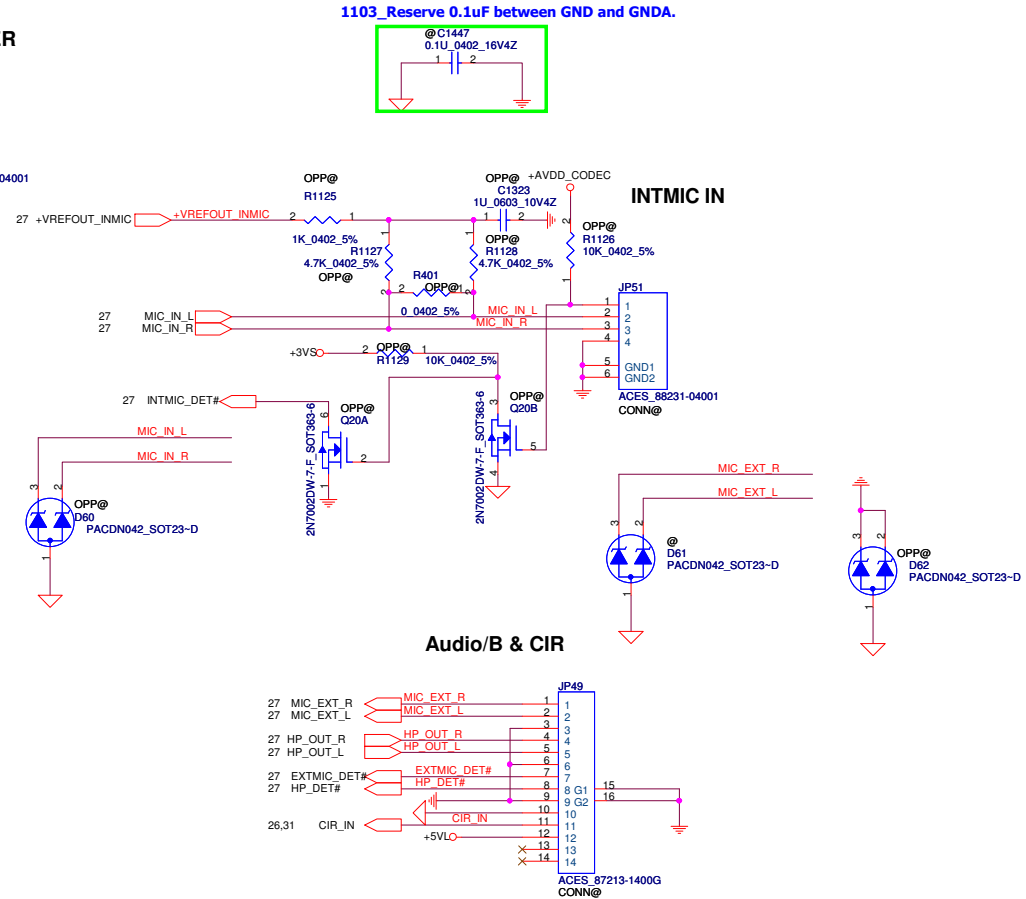
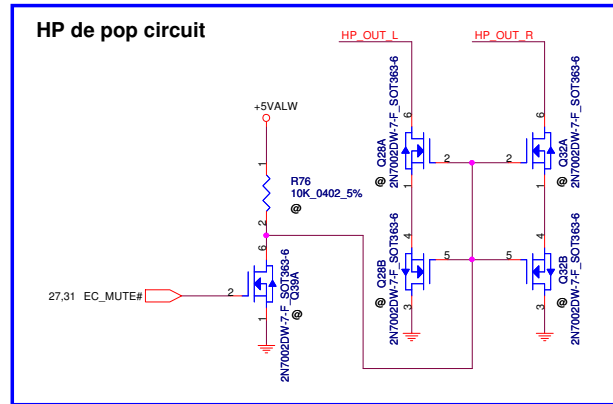
MDC 1.5 Conn.



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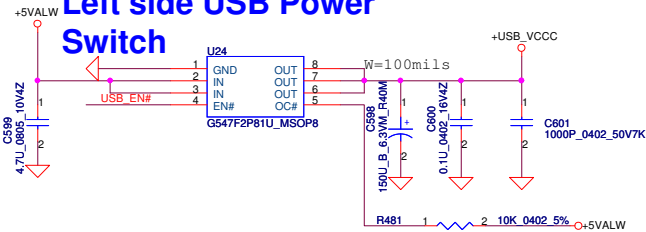


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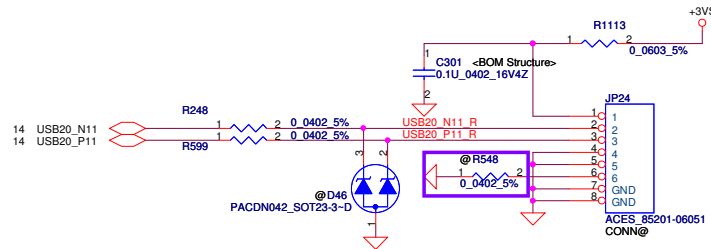


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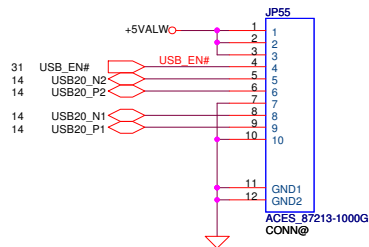
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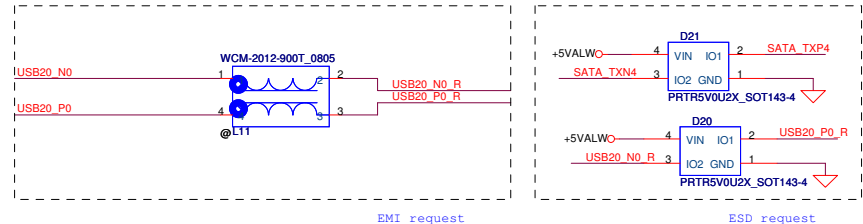
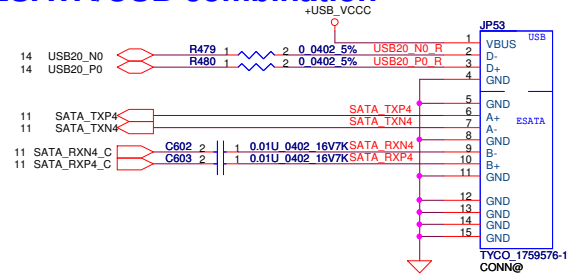
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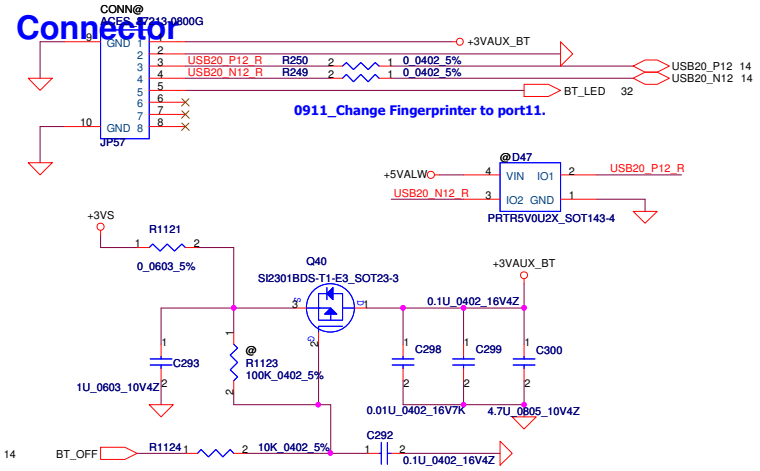
USB cable connector for Right side



Left\ side ESATA/USB combination Connector

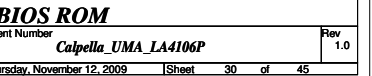


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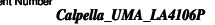


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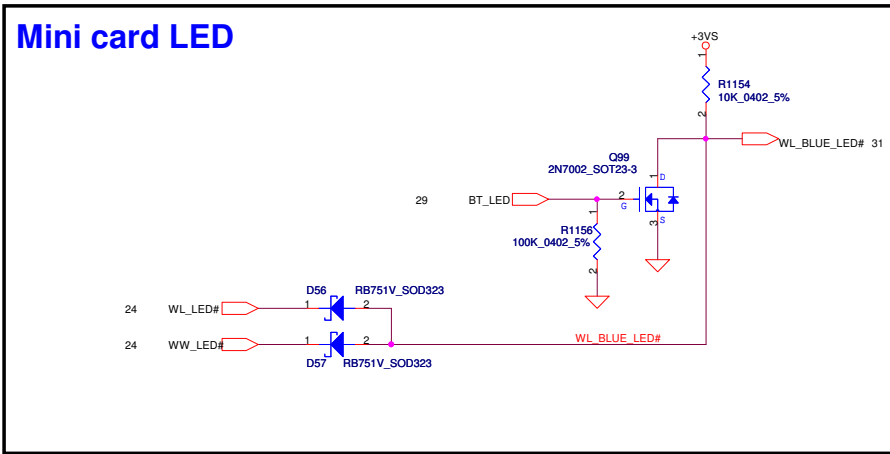
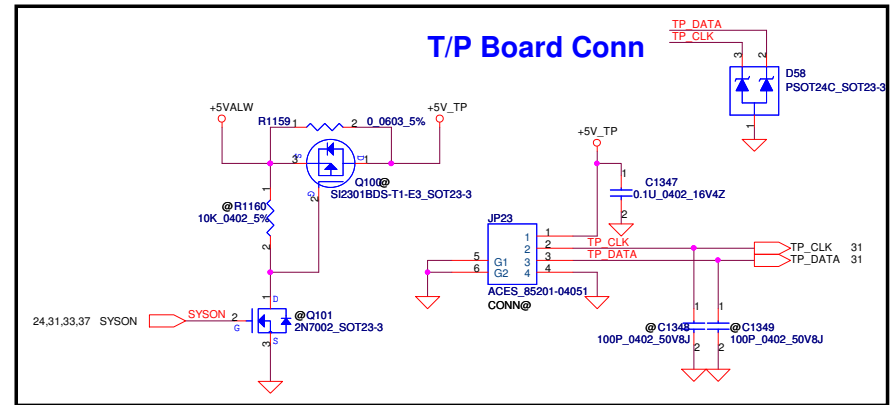
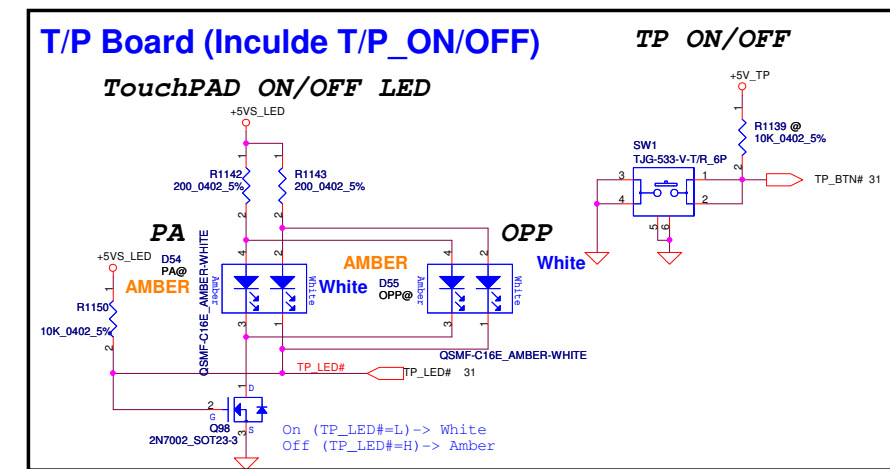
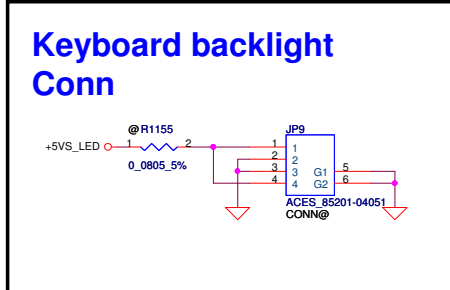
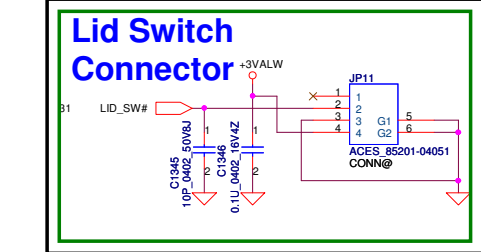
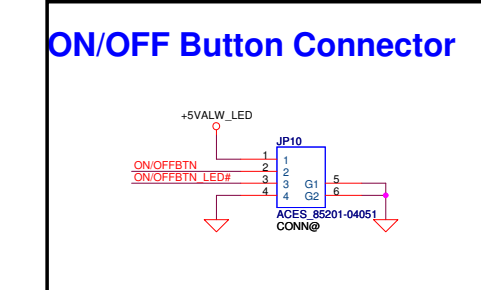
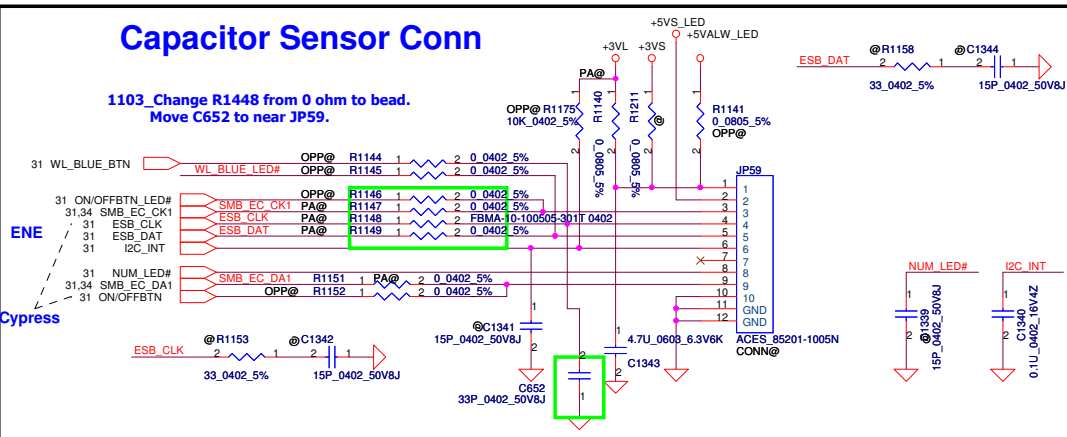
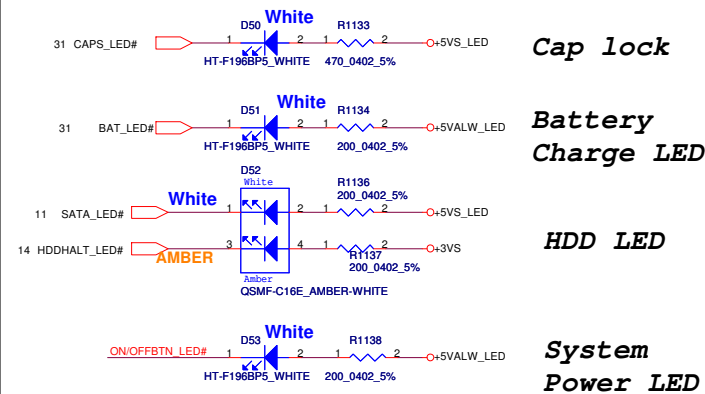



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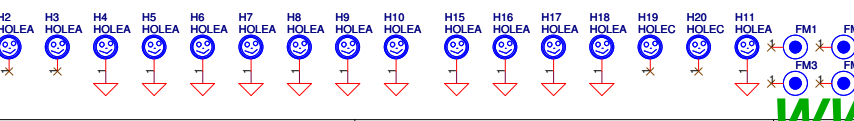
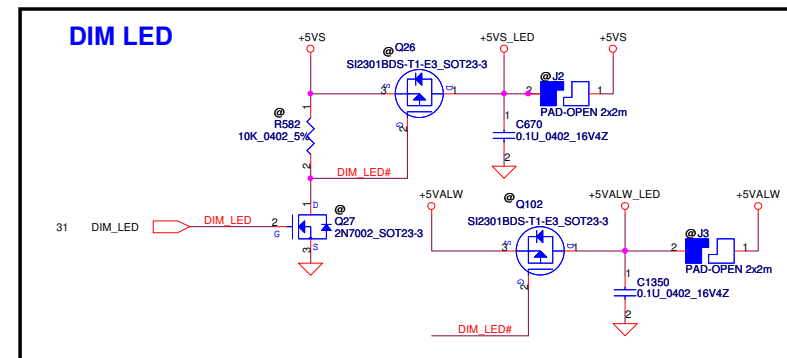
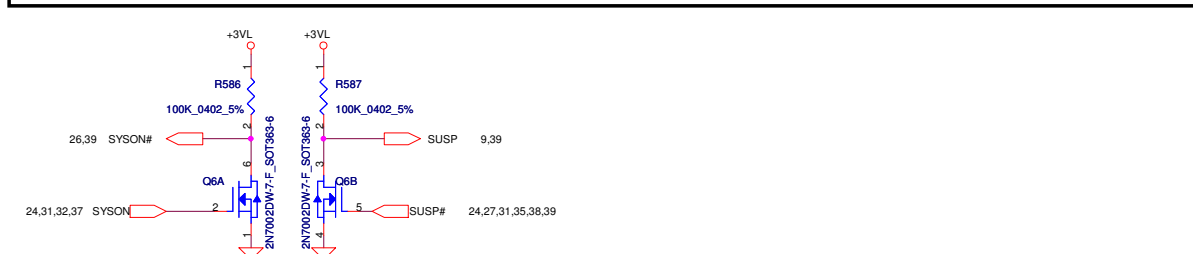
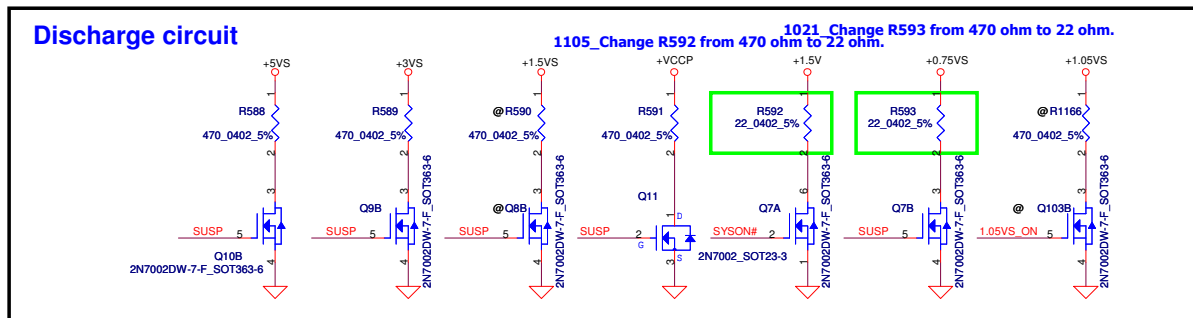
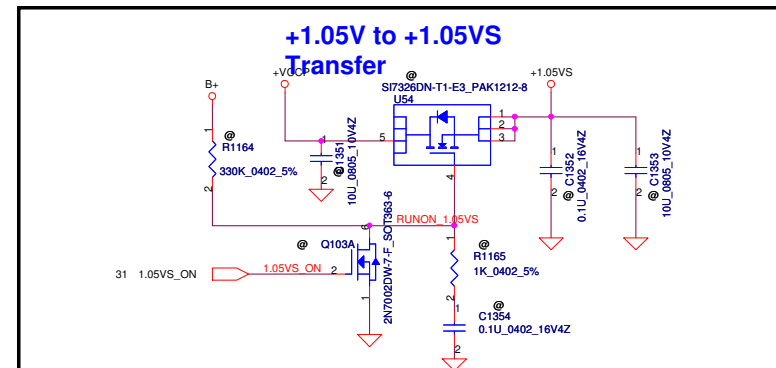
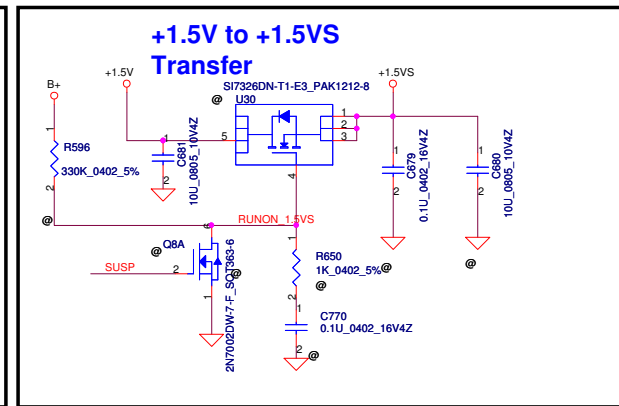
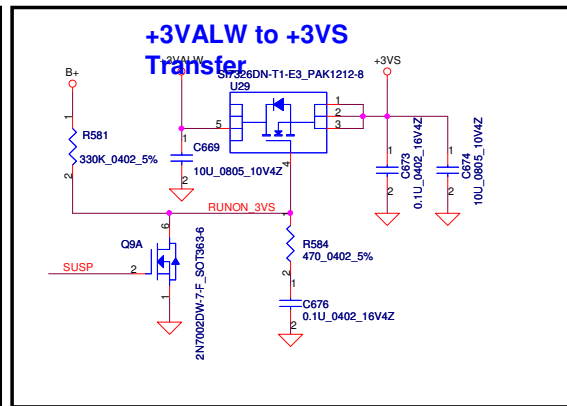
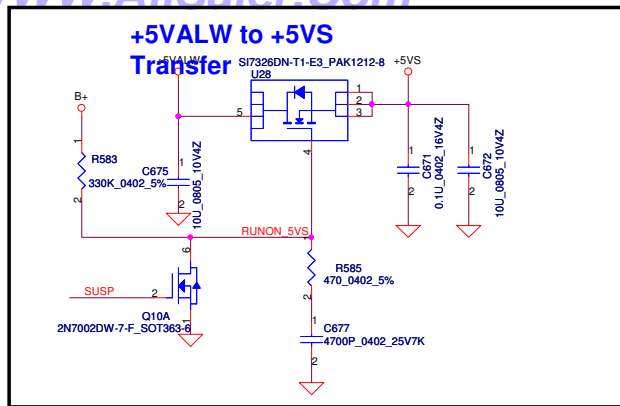


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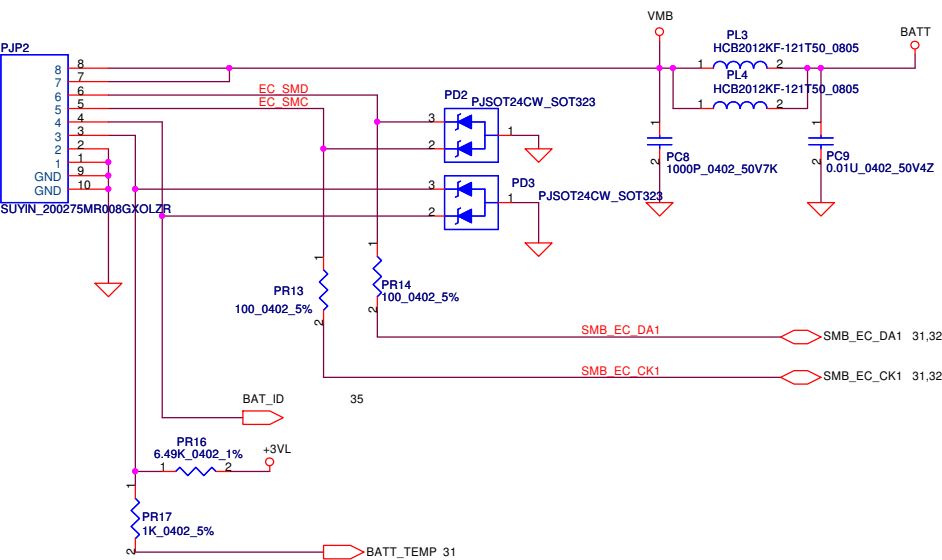
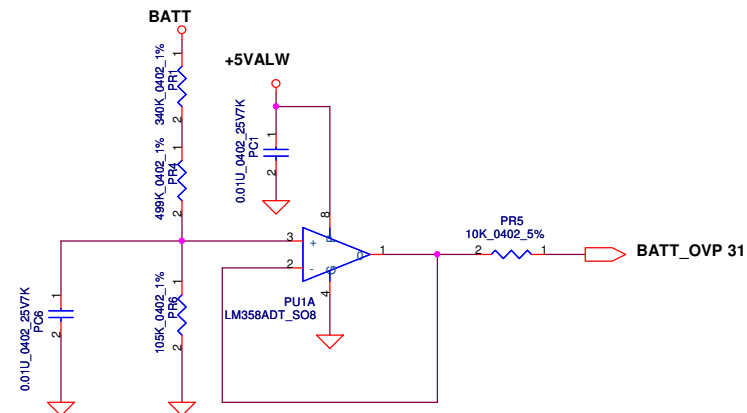
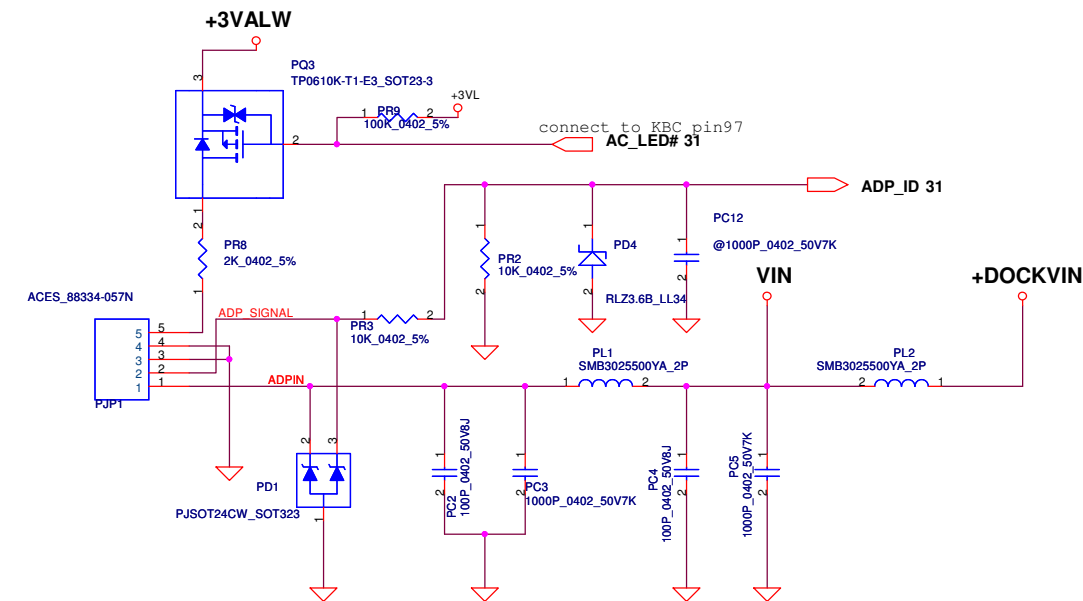




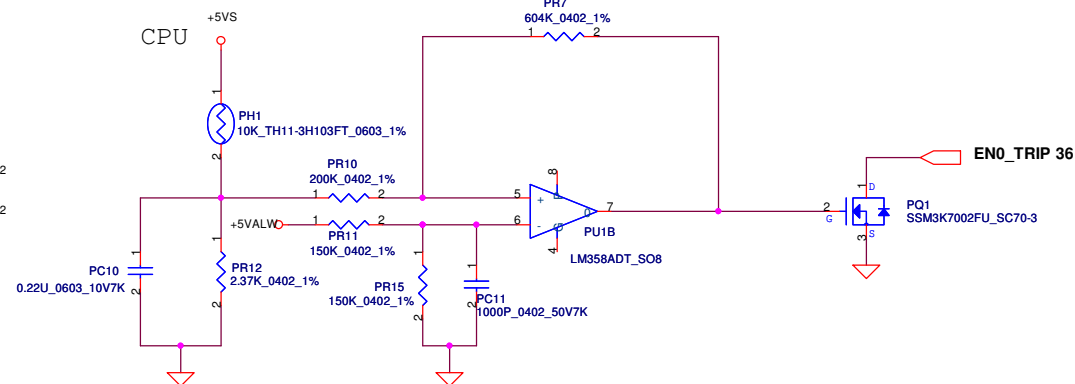
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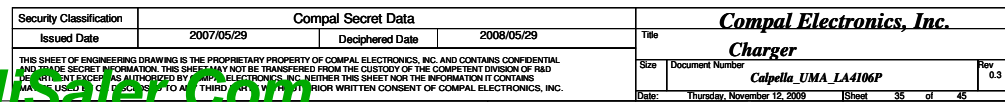
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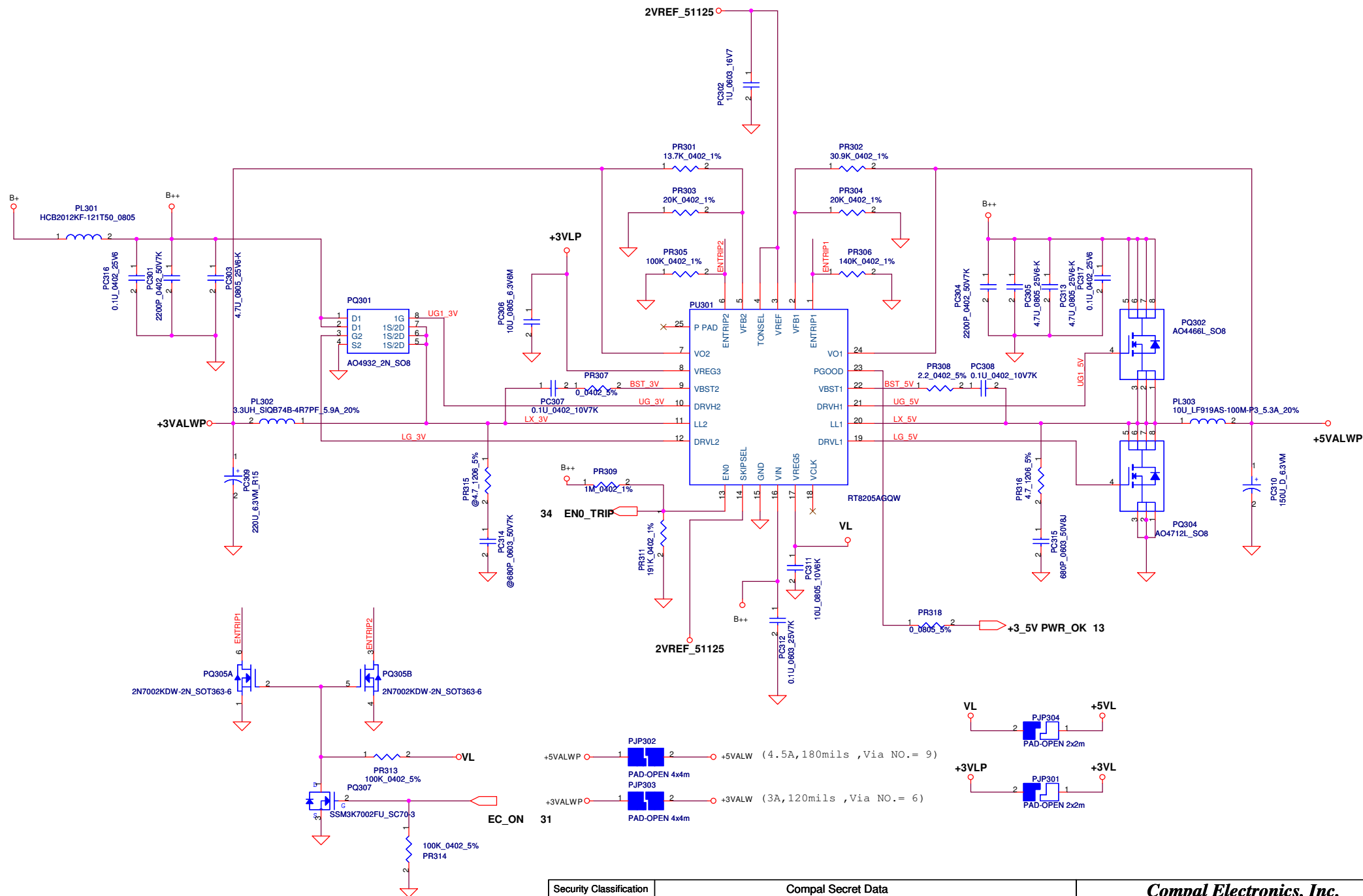


PH1 under CPU bottom side :
CPU thermal protection at 90 \pm 3 degree C

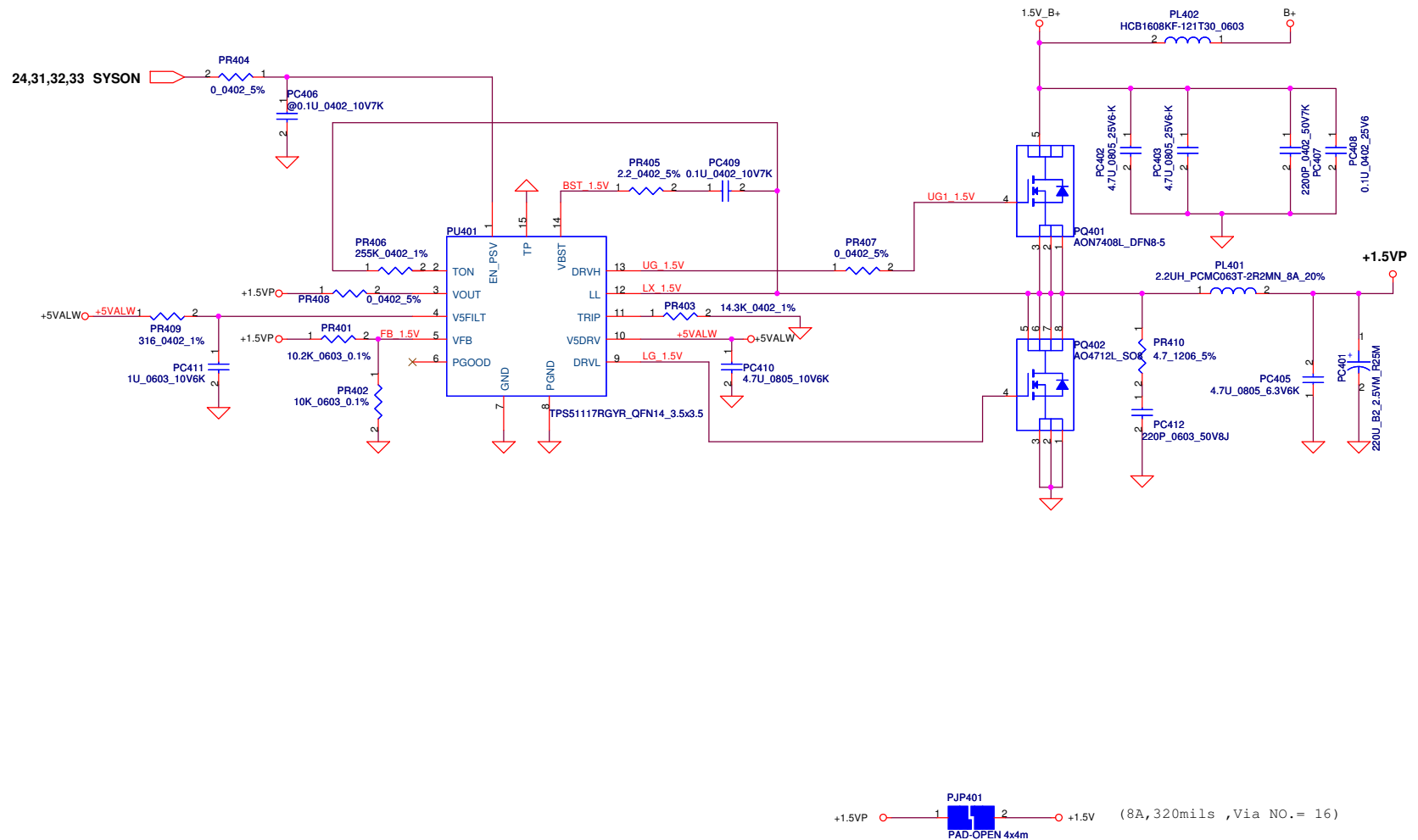


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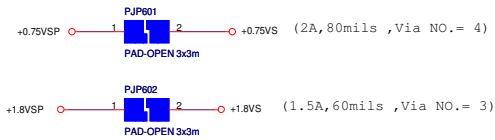
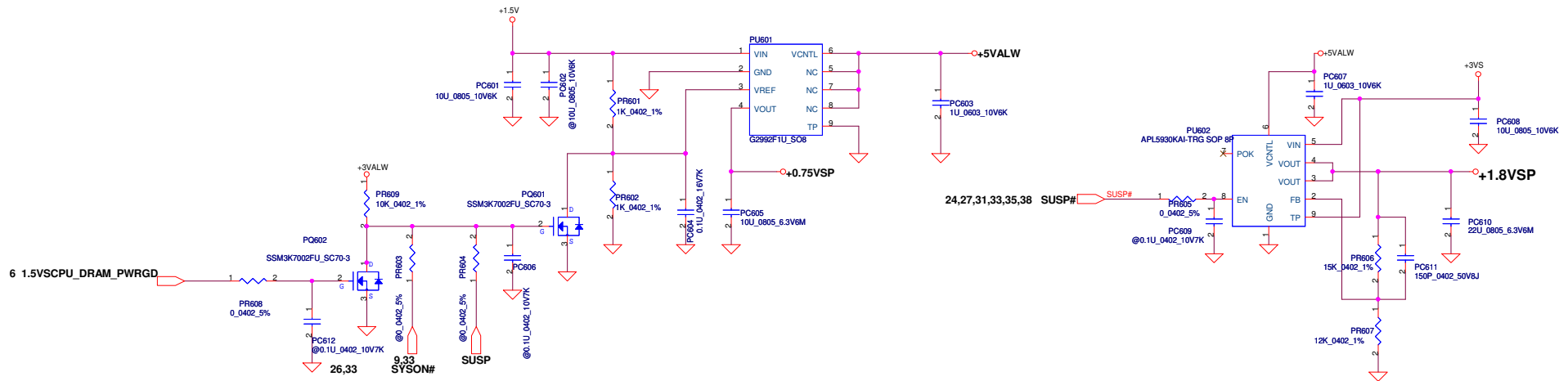


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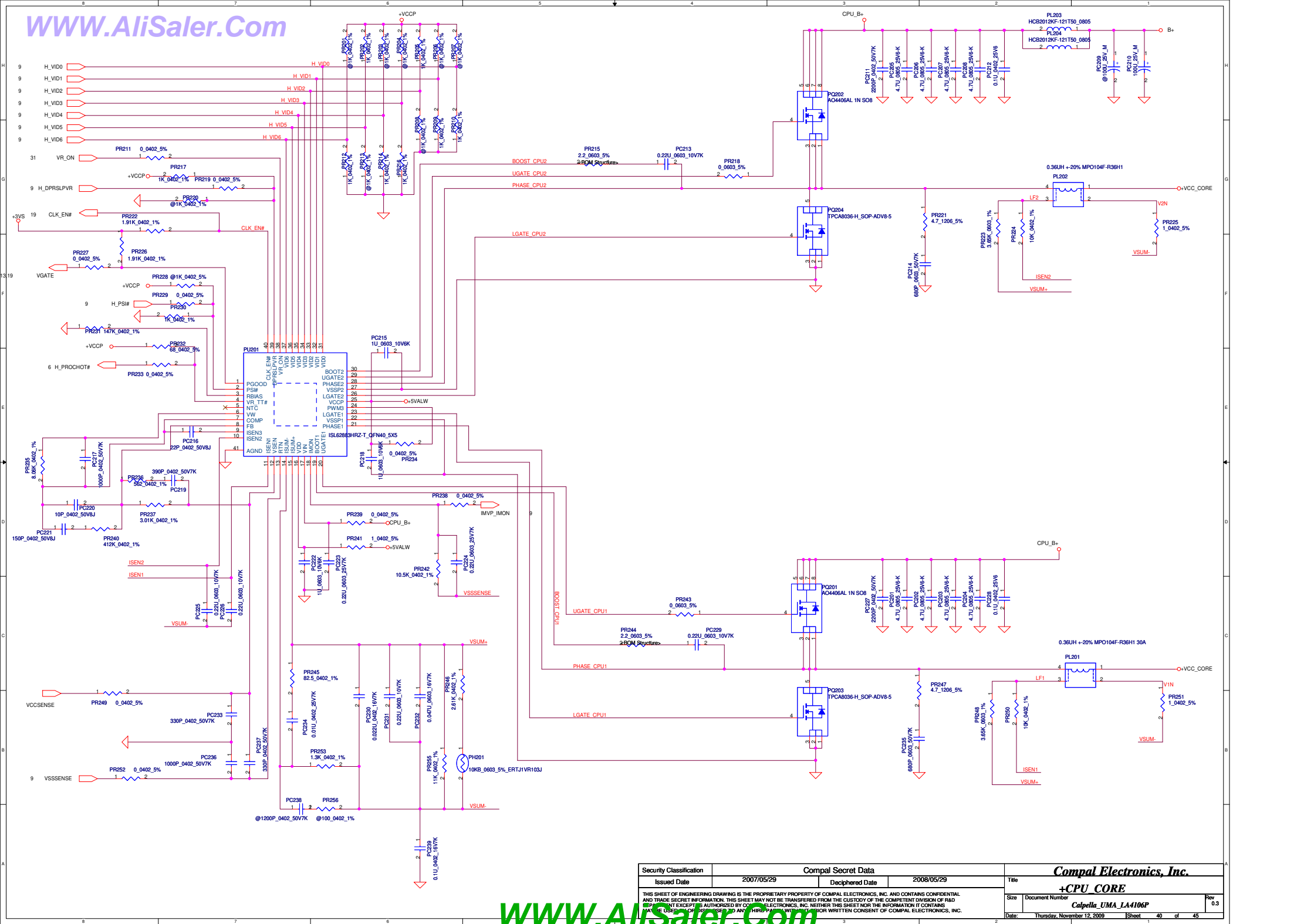


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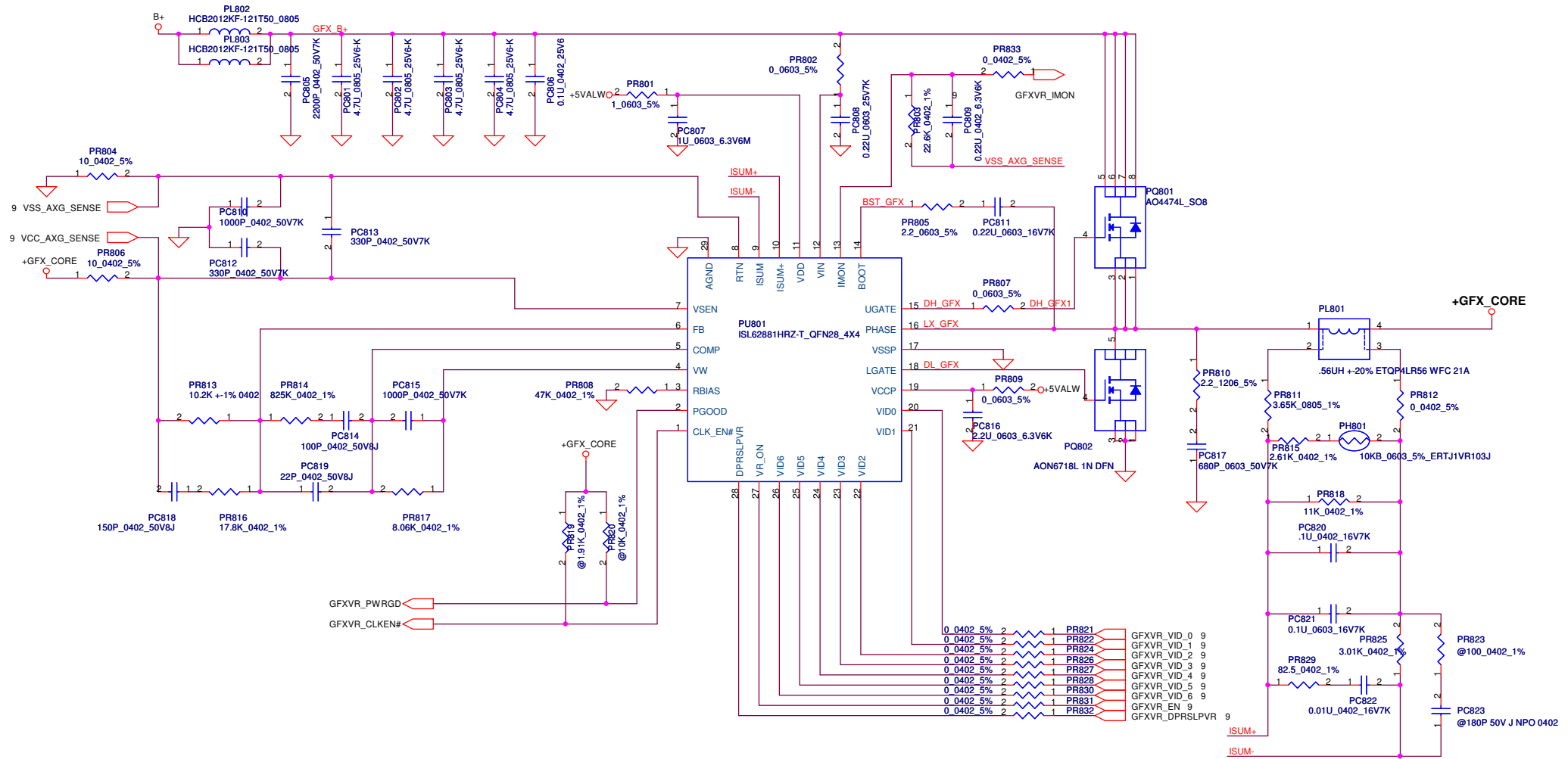
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Item	PAGE	Fixed Issue	Request by	Modify List	Date	Note
01	22		HW	Add R801	7/20.	DB --> PV-1
02	26	Fix Volum up/down cannot work on Docking.	HW	Add R1185, R1186 and pull high to +3VS.	7/20.	DB --> PV-1
03	31	Remove double pull high resistor.	HW	Delete R660.	7/20.	DB --> PV-1
04	13	Per EMI request.	EMI	Change R679 from 33 ohm to 100 ohm.	7/20	DB --> PV-1
05	31	Modify correct pull high resistor value.	HW	Change R512 and R513 from 4.7K to 2.2K ohm.	7/20	DB --> PV-1
06	32	Modify LVDS PWM connection.	HW	Connect R890 to PCH and R505(reserve) to EC.	7/24	DB --> PV-1
07	22	Fix cannot hot plug if use Asmedia level shifter.	HW	Remove R862 and R867.	8/13	DB --> PV-1
08	22	Add series for Express card delete signal between Express card power swtich and PCH For Board ID.	HW	Add R1210	8/13	DB --> PV-1
09	31		HW	Add R386 and pull low to GND.	8/13	DB --> PV-1
10	31	Change LAN power off control pin to U27 pin115.	HW	Connect U27 pin115 and add series resistor R543 to LAN power control circuit.	8/13	DB --> PV-1
11	31	Change LID switch power rail from +3VL to +3VALW.	HW	Pull high R526 to +3VALW.	8/13	DB --> PV-1
12	31	Delete useless parts.	HW	Delete R542 because already connect EC_UTX to MINI PCIE connector	8/13	DB --> PV-1
13	32	Change LID switch power rail from +3VL to +3VALW.	HW	Change JP11 pin 1 to +3VLALW.	8/13	DB --> PV-1
14	33	For Cost down.	HW	Reserve U30, R596, R650, R590, C681, C770, C679, C680, Q8; add PJ2 to connect +1.5VS_CPU and +1.5VS power plan.	8/13	DB --> PV-1
15	33	Try to use +1.5VS to replace +1.8VS power rail.	HW	Add and reserve PJ3 to short +1.8VS and +1.5VS_CPU power plan.	8/13	DB --> PV-1
16	14	Modify prevent S3 leakage issue circuit.	HW	Connect PCH_DDR_RST from EC GPIO48 to PCH GPIO46.	8/13	DB --> PV-1
17	31	Modify prevent S3 leakage issue circuit.	HW	Delete R386	8/13	DB --> PV-1
18	21	Fix LCD panel no display issue.	HW	Connect JLVDS1 pin27 to +3VS.	8/13	DB --> PV-1
19	32	Change Cap. board power rail from +3VL to +3VS.	HW	Reserve R1211 and connect to +3VS.	8/13	DB --> PV-1
20	27	Swap Audio port A and F.	HW	Swap port A and port F. Detail please see audio circuit.	8/17	DB --> PV-1
21	6	Delete XDP connector	HW	Delete JP1, R13, R17, R18, R19, R22, R25, C1	8/17	DB --> PV-1
22	25	Conecto Q15 to +3V_LAN.	HW	Delete R1031 and connect Q15 pin1 to +3V_LAN directly.	8/17	DB --> PV-1
23	26	Modify Audio circuit near docking side.	HW	Connect Q91 pin3 to GNDA and move it near Codec.	8/17	DB --> PV-1
24	27	Per EMI/ESD request.	EMI/ESD	Add R1212/C1433 for HDA_RST#_CODEC. Add C1434. Change R132/R135/R139 to C1435/C1436/C1437.	8/17	DB --> PV-1
25	6	Modify prevent S3 leakage issue circuit.	HW	Change U57 from reset IC to AND gate; add R1218 and reserve R383; add voltage divider(R1216/R1217) for VTPWRGOOD.	8/19	DB --> PV-1
26	25	Follow DIS.	HW	Change Y8 material.	8/19	DB --> PV-1
27	28	Per ESD request.	ESD	Add D61, D62 for OPP sku.	8/19	DB --> PV-1
28	32	Change cap. board power rail from +3VL to +3VS.	HW	Pull high R544 and R545 to +3VS power rail.	8/20	DB --> PV-1
29	14	Make sure PLT_RST# level is stable.	HW	Stuff R185.	8/20	DB --> PV-1
30	32	Reserve +3VL power rail for cap. board.	HW	Add and reserve R1219/R1220 to +3VL.	8/21	DB --> PV-1

Item	PAGE	Fixed Issue	Request by	Modify List	Date	Note
01	6	Make sure +1.5VS can ramp up early than +0.75VS.	HW	Connect 1.5VSCPU_DRAM_PWRGD to enable PU601.	9/11	PV-1 --> PV-2
02	11	ME fuction control enable/disable.	SW/EC	Add Q106, R1221, R1222 and connect to EC pin26.	9/11	PV-1 --> PV-2
03	13	For support ME function.	SW/EC	Connect SUS_PWR_ACK to EC pin76.	9/11	PV-1 --> PV-2
04	14	HM55 disable USB port6/port7.	INTEL	Change Bluetooth port6 to port12, change Fingerprinter port7 to port11.	9/11	PV-1 --> PV-2
05	27	To solve no Vref out when external MIC change from port A to port F.	HW	Reserve R431, add R and connect to +AVDD_CODEC.	9/11	PV-1 --> PV-2
06	27	Delete EC_BEEP from EC because useless.	HW	Delete EC_BEEP to EC.		
07	28	Delete ANA_MIC_DET net to EC.because useless.	HW	Delete ANA_MIC_DET to EC.	9/11	PV-1 --> PV-2
08	29	HM55 disable USB port6/port7.	INTEL	Change Bluetooth port6 to port12, change Fingerprinter port7 to port11.	9/11	PV-1 --> PV-2
09	31	Board ID is not enough when use pin81.	EC	Swap TP_BTN# and BDID, then add pull high resistor R1223 for BDID.	9/11	PV-1 --> PV-2
10	31	ME fuction control enable/disable.	SW/EC	Remove EC_BEEP and change to ME_EN, then connect ME_EN to Q106.	9/11	PV-1 --> PV-2
11	31	For support ME function.	SW/EC	Remove ANA_MIC_DET and change to SUS_PWR_ACK, then connect SUS_PWR_ACK to PCH.	9/11	PV-1 --> PV-2
12	31	Chagne ENE cap. board ESB bus power rail from +3VS to +3VL.	HW	Reserve R544/R545 and stuff R1219/R1220.	9/11	PV-1 --> PV-2
13	32	Chagnge Cap. board power rail from +3VS to +3VL.	HW	Reserve R1211 and stuff R1140.	9/11	PV-1 --> PV-2
14					9/11	PV-1 --> PV-2

